Laser Reliability and Defects

Mater. Res. Soc. Symp. Proc. Vol. 1432 © 2012 Materials Research Society
DOI: 10.1557/opl.2012.902

Highly Reliable 1060nm Vertical Cavity Surface Emitting Lasers (VCSELs) For Optical Interconnect

S. Kamiya[1], K. Takaki[2], S. Imai[2], J. Yoshida[2], M. Funabashi[2], Y. Kawakita[2], K. Hiraiwa[2], T. Suzuki[2], H. Shimizu[2], N. Tsukiji[2], T. Ishikawa[1], and A. Kasukawa[2]
[1]Reliability First Group, Furukawa Electric Co., Ltd., Yokohama, Japan
[2]Photonic Device Research Center, Furukawa Electric Co., Ltd., Ichihara, Chiba, Japan

ABSTRACT

High reliability, low power consumption and high speed laser diodes are required for optical interconnect. We developed 1060nm VCSELs with InGaAs/GaAs strained quantum wells, oxide-confined and double intra-cavity structures for that purpose. As for the power consumption, low power dissipation of 0.14 mW/Gbps at 10 Gbps operation has been achieved. Clear eye openings up to 20 Gbps were confirmed at a low bias current of 5 mA. In the reliability test, accelerated aging tests were performed up to 5,000 hours at 6 mA in three different temperatures, 70 ^{o}C, 90 ^{o}C and 120 ^{o}C. The total number of the VCSELs was 4,898 pcs (approximately 5,000). No failure was observed. Under the normal operating condition of 40 ^{o}C and 6 mA, the total device-hours was 7.75×10^{7} hours assuming Ea = 0.35 eV according to Telcordia GR-468-CORE. The random failure rate of 30 FIT with the confidence level (C.L.) of 90 % and 12 FIT with the C.L. of 60 % were estimated. To estimate the wear-out lifetime and the number of FITs, high stressed aging tests with 170 ^{o}C and 6 mA were performed. With the acceleration factor of Ea = 0.7 eV in the wear-out failure, the median lifetime was 3,000 hours which was equivalent to 300 years in 40 ^{o}C ambient. The FIT numbers due to the wear-out were estimated as 0.3 FIT for 10 years. Compared with the random failure rate of 30 FIT, the wear-out failure rates are considered to be negligible. In the extremely long term aging test with 90 ^{o}C and 6 mA, no wear-out trend has been observed in both threshold current and optical power up to 20,000 hours operation. These results indicate that 1060 nm VCSEL is promising light source used in optical interconnect for high performance computers and data centers.

INTRODUCTION

The performance for data centers and super computers is increasing. According to the performance chart in high performance computing (HPC) system, the performance growth has been projected by a factor of 10 times in every 4 years, so the requirement of system bandwidth is increased[1-3]. Optical interconnect becomes more important for its advantage of higher bandwidth, higher transmission speed and lower power consumption compared to electrical wire interconnect. Optical interconnects have been installed in rack-to-rack, board-to-board, or chip-to-chip data transfer of large systems. Much larger number of channels is needed in the large systems than usual optical communication. Therefore, high reliability, low power consumption and high speed laser diodes are required for optical interconnects.

Vertical cavity surface emitting lasers (VCSELs) are mainly employed as light sources and play a key role to further improve the performances of optical interconnects. Especially, low power consumption, highly reliable, and high speed operations are essential, and these must be realized simultaneously in commercial devices.

Figure 1 shows our 1060nm VCSEL with InGaAs/GaAs strained quantum wells, oxide-confined and double intra-cavity structures. As for the power consumption, low power dissipation of 0.14 mW/Gbps at 10 Gbps operation has been achieved[4,5]. Clear eye openings up to 20 Gbps were confirmed at a low bias current of 5 mA.

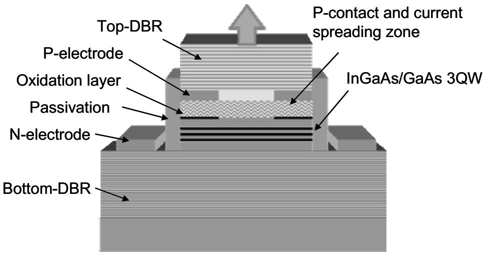

Figure 1: Schematic of VCSEL structure

As described above, large number of optical interconnects is necessary in high performance computers and data centers. Therefore, very high reliability is required of a single chip VCSEL. In order to verify reliability properties of our VCSELs, we performed several reliability tests.

EXPERIMENT

Accelerated aging tests were performed in configuration of 20-pin dual in-line package (DIP). VCSEL arrays were assembled under non-hermetic atmosphere. Before the assembly, the L-I characteristics of all chips were measured on-wafer and the chips with characteristics failures were determined. Then all chips were screened through on-wafer burn-in process in order to eliminate infant mortalities. After the burn-in process, the wafer was divided into arrays and assembled onto the DIPs. Then all DIPs were screened through burn-in process again in order to eliminate ESD failures. After the DIP burn-in, the L-I characteristics were checked again, and then the high temperature aging tests were initiated. The DIP samples on test boards were put in a thermostatic chamber during the aging period, and L-I characteristics were measured outside of the thermostatic chamber at certain intervals. The chip failure or End-of-Life was defined as the time when the laser optical power showed 2 dB degradation from its initial value under 6 mA at room temperature.

DISCUSSION

Random Failure

To estimate the random failure rate, the aging tests were performed in three different temperature conditions. Table 1 shows the detail information of ambient temperature, number of chips, aging time, device-hours and number of failures.

Cambridge University Press
978-1-605-11409-5 - Materials Research Society Symposium Proceedings Volume 1432: Reliability and Materials Issues of III-V and II-VI Semiconductor Optical and Electron Devices and Materials II
Editors Osamu Ueda, Mitsuo Fukuda, Kenji Shiojima and Edwin Piner
Excerpt
More information

Table 1: Accelerated Aging Tests

Condition (Ambient temperature, bias current)	Quantity (number of chips)	Maximum aging duration (hours)	Device hours @40°C, 6mA	Number of failures
70°C, 6mA	1,075	5,000	8.0×10^6	0
90°C, 6mA	1,121	5,000	1.6×10^7	0
120°C, 6mA	2,702	2,000	5.4×10^7	0
Total	4,898		7.8×10^7	0

The aging tests were performed up to 5,000 hours at 6 mA in 70 °C and 90 °C, and up to 2,000 hours at 6 mA in 120 °C. The duration of 90 °C and 120 °C was determined for 30 years operation in 40 °C with the acceleration factor of acceleration factor of Ea = 0.7eV as described in papers[6-9]. In this study, the total number of the VCSELs was 4,898 pcs (approximately 5,000), and no failure was observed. Time dependencies in change ratio of optical power for the longest aged lot are shown in Figure 2.

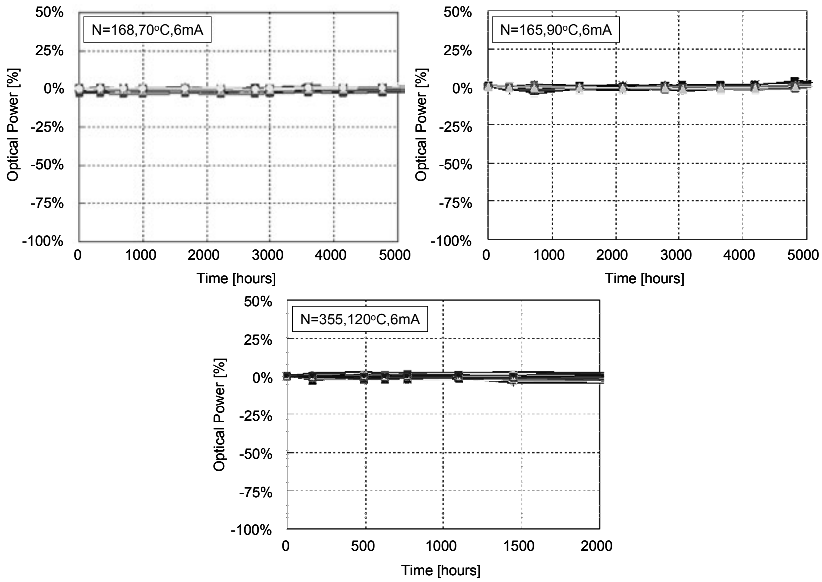

Figure 2: Time dependencies in change ratio of optical power for the longest aged lot

Assuming the normal operating condition of 40 °C and 6 mA, the total device-hours was 7.75×10^7 hours with the activation energy (Ea) of 0.35 eV and no current accelerated factor in calculation according to Telcordia GR-468-CORE. The number of Failure in term (FIT) is calculated. The random failure rate of 30 FIT with the confidence level (C.L.) of 90 % and 12 FIT with the C.L. of 60 % were estimated.

Wear-out

In order to estimate the wear-out lifetime and the number of FITs, the high stressed aging test with 170 °C ambient temperature and 6 mA bias was performed. The aging data and the Weibull plot estimated from the fitting curve are shown in Figure 3.

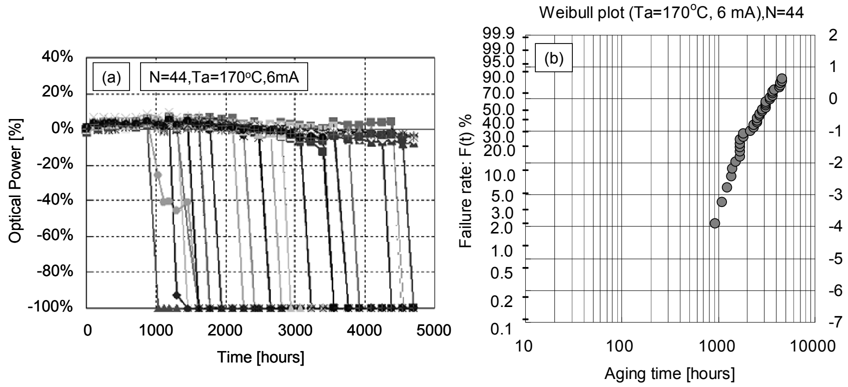

Figure 3 (a) High stressed aging test results at 170 oC and 6mA. (b) Weibull plot from the wear-out test in (a).

All failure modes were analyzed and confirmed as the dislocation at the oxidation front region as reported. With the acceleration factor of Ea = 0.7 eV in the wear-out failure and the junction temperature of 190 °C, the median lifetime was 3,000 hours which was equivalent to 300 years in 40 °C ambient. The FIT numbers due to the wear-out were estimated as 0.3 FIT for 10 years and 1.1 FIT for 20 years. Compared with the random failure rate of 30 FIT, the wear-out failure rates are considered to be negligible.

The extremely long term aging test with 90 °C ambient temperature and 6 mA for the previous lot were performed. The differences between the previous and current design are slight such as the thickness of the electrode, therefore the reliability levels for both designs can be considered quite similar. The total number of tested VCSELs was 172 pcs. Time dependencies in change ratio of optical power and threshold current are shown in Figure 4. No degradation trend has been observed in both optical power and threshold current up to 2.3 years (20,000 hours) operation. The duration is equivalent for 60 years operation in 40 °C.

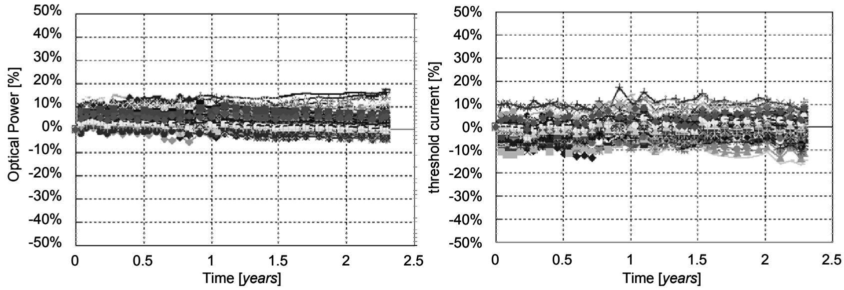

Figure 4: Extremely long term aging test with 90 ^{o}C, 6 mA (N=172)

Endurance Tests

VCSEL arrays are often used in non-hermetic ambient, so endurance tests in bare chips should be performed. Table 2 shows the results of five kinds of endurance tests performed under non-hermetic atmosphere according to the procedure on Telcordia GR-468 Issue 2. For all of endurance tests, the change ratio of the optical power was within ±20%, so all tests were passed.

Table 2: endurance tests

Test	Test Condition	Quantity (chips)	Criteria	Pass/Fail
High Temperature Storage	85 ^{o}C, 2,000 hours	39	Po < ±20%	Pass
Low Temperature Storage	-40 ^{o}C, 72 hours	40	Po < ±20%	Pass
Damp Heat	85 ^{o}C/85%RH, 500 hours	39	Po < ±20%	Pass
Temperature Cycle	-40°C/+85°C, 50 cycles	38	Po < ±20%	Pass
Damp Heat Aging	85 ^{o}C/85%RH, 2000 hours, Ith ×1.2	65	Po < ±20%	Pass

CONCLUSIONS

The random failure rate estimated by the aging tests, at three temperature conditions with 4,898 VCSEL chips, was 30 FIT at C.L. = 90 % under the operating condition of 40 ^{o}C and 6 mA. No degradation of threshold current and optical power was observed during their wear-out lifetime, and the results would support the stable 10 Gbps operation over life. Also the change ratios of the optical power were within criteria in endurance tests. As the results mentioned above, the Furukawa's 1060 nm VCSEL chips can operate at 10 Gbps modulation in non-hermetic atmosphere with high reliability. It indicates that 1060 nm VCSEL is promising light source used in optical interconnect for high performance computers and data centers.

REFERENCES

1. J. A. Kash, A. F. Benner, F. E. Doany, D. M. Kuchta, B. G. Lee, P. K. Pepeljugoski, L. Schares, C. L. Schow and M. Taubenblatt., "Optical Interconnects in Exascale Supercomputers," Proc. Photonics Society 23rd annual meeting, WR1 (2010)
2. www.top500.org
3. www.green500.org
4. S. Imai, K. Takaki, S. Kamiya, H. Shimizu, J. Yoshida, Y. Kawakita, T. Takagi, K. Hiraiwa, H. Shimizu, T. Suzuki, N. Iwai, T. Ishikawa, N. Tsukiji and A. Kasukawa, "Recorded Low Power Dissipation in Highly Reliable 1060-nm VCSELs for "Green" Optical Interconnection", IEEE J. Sel. Top. Quant. Electron., vol. 17, No. 6, 1614-1620, (2011).
5. S. Imai, K. Takaki, H. Shimizu, Y. Kawakita, T. Takagi, K. Hiraiwa, H. Shimizu, N. Iwai, N. Tsukiji, and A. Kasukawa., "Recorded Low Power Dissipation of 0.14mW/Gbps in 1060nm VCSELs for "Green" Optical Interconnection,", Proc. 22nd ISLC, 174-175, (2010).
6. N. –Y. Li, D. Collins, S. Jatar, O. Lavrova, C. Helms, W. Luo, L. Liu, C. Liu, M. Qiu, K. Roff and C. Wang., "Design and Manufacturing of 10G GenX VCSELs at Emcore," Proc. SPIE 6484, 648402-1-11, (2007)
7. J. K. Guenter, J.A. Tatum, R.A. Hawthorne III, R. H. Johnson, D. T. Mathes and B. M. Hawkins, "A plot twist: the continuing story of VCSELs at AOC," Proc. SPIE 5737, 20-34, (2005)
8. D.W. Kisker, L. M. F. Chirovsky, R. L. Naone, J. M. Van Hove, J. M. Rossler, M. Adamcyk, N. Wasinger, J. G. Beltran and D. Galt., "1.3µm VCSEL production issues," Proc. SPIE 5737, 146-157, (2004)
9. D. Wiedenmann, M. Grabherr, R. Jager and R. King., "High volume production of singlemode VCSELs", Proc. SPIE 6132, 613202-1-12, (2005)

Cambridge University Press
978-1-605-11409-5 - Materials Research Society Symposium Proceedings Volume 1432: Reliability and Materials Issues of III-V and II-VI Semiconductor Optical and Electron Devices and Materials II
Editors Osamu Ueda, Mitsuo Fukuda, Kenji Shiojima and Edwin Piner
Excerpt
More information

Mater. Res. Soc. Symp. Proc. Vol. 1432 © 2012 Materials Research Society
DOI: 10.1557/opl.2012.903

Design for Reliability and Common Failure Mechanisms in Vertical Cavity Surface Emitting Lasers

Robert W. Herrick[1]
[1]JDSU Inc, 80 Rose Orchard Way, San Jose, CA 95134, U.S.A.

ABSTRACT

Vertical-Cavity Surface-Emitting Lasers are making up a large and growing share of the world's production of semiconductor lasers. But the 850 nm GaAs quantum well VCSELs that make up most of present product are highly vulnerable to dislocation networks. In this paper, we discuss how materials selection affects the reliability of semiconductor lasers generally. We then describe the most common failure mechanisms observed in VCSELs, and what precautions are used to prevent them. We finish with a brief discussion of reliability testing and failure analysis.

INTRODUCTION

Vertical Cavity Surface Emitting Lasers (VCSELs) are one of the most popular types of semiconductor lasers, and command a large and increasing market share over the past several years. It is estimated that approximately 700 million VCSELs have been sold [1] in the 15 years since they have been commercialized, with some estimates ranging as high as one billion VCSELs sold. The three primary applications are as a light source for data communications in short-reach fiber optic transceivers, as an illumination source for optical mice, or as an illumination source for thumb trackpads on cell phones. For these latter two applications, VCSELs are the least expensive semiconductor laser made, with costs in volume that are said to be roughly U.S. $0.12 per VCSEL.

The traditional semiconductor laser dates back to the 1970's for serious commercialization, and emits out cleaved facets, as shown in Figure 1 below. By contrast, the modern VCSEL is a more recent development, dating to the 1990's for commercialization; it has the light travel perpendicular to the plane of the active region. In addition to low cost, other advantages of VCSELs include lower pumped area that in turn means lower required drive current or power consumption; the VCSEL also has a round, stigmation-free beam that makes for simpler collimation optics. Disadvantages of VCSELs include high thermal resistance, a more limited range of available wavelengths (only 650-1070nm commercially available as of this writing), and limited power per unit area.

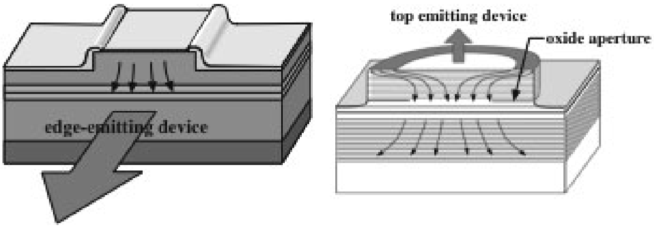

Figure 1: Edge-emitting lasers (left) have light that travels in the plane of the active region, and bounces between the front and back facet before being emitted. In VCSELs (right) the light goes up and down, perpendicular to the plane of the active region.

CONSIDERATIONS FOR MATERIALS SELECTION FOR SEMICONDUCTOR LASERS

With any semiconductor laser, the choice of "materials system" is key. By "materials system, we primarily mean the choice of the substrate to grow the laser on, and the alloys used to make the laser. Especially important is the material of the quantum wells used to create light, and the barriers that contact the wells.

Discussion of materials selection is usually retrospective: after a material is widely adopted commercially, or rejected by researchers abandoning it, perhaps people try to explain why it was or wasn't successful (e.g., "the material was too soft, and thus allowed easy dislocation propagation"). Or perhaps they use general rules such as "adding indium to the quantum well improves lifetime, while adding aluminum makes it worse." However, it is often possible to predict early on how suitable a material will be with a few easy tests, or perhaps even with theoretical calculations. In the following section, we wish to introduce two concepts that are not widely known. First, not many people are familiar with the issue of whether dangling bonds from crystal imperfections create mid-gap trap states (undesirable) or whether they create trap states in the valance or conduction band (which is far less dangerous). Second, the mechanism for dislocation pinning in compressively strained quantum wells is widely misunderstood, so we will discuss the most plausible explanation.

Any mechanical damage that might occur with the laser, damage from electrostaic discharge (ESD), and many types of crystal defects, will all result in "dangling bonds" – i.e., atoms in the lattice that are missing a neighbor, and thus are not covalently bonded in the normal fashion. In many laser materials, such dangling bonds result in mid-gap trap states, which in turn result in self-propagating climb dislocation networks that can rapidly kill semiconductor lasers when they become damaged. The vulnerability of lasers to maverick (random) failure is highly dependent on such dislocation network growth.

Fundamentally, there are three classifications that can be made for semiconductor laser materials systems. We list them in order of descending preference.

Category 1: Materials where dangling bonds do *not* result in mid gap trap states. This is the most desirable laser type, as it is much less vulnerable to maverick failure. Examples include InGaAsP lattice matched to InP (1.3µm or 1.55µm) or InGaN grown on C-plane GaN (400-