1 Introduction

Current technology is progressing fast towards the development of low-cost and high-performance processes for the fabrication of large-area electronic (LAE) applications on both rigid and flexible/stretchable substrates, including flexible field effect transistors (FETs) [1–6], thin film transistors (TFTs) [7, 8], transparent flexible LAE devices [7, 9], flexible tactile *e*-skin [10–15], smart-coatings for photovoltaics [16, 17], flexible patches for health monitoring [18-24], flexible metal-semiconductor-metal (MSM) LAE devices [25], flexible optoelectronics [26, 27], stretchable conductive interconnects [28] and flexible integrated circuits (ICs) [29, 30]. The compatibility of LAE device fabrication processes with roll-to-roll (R2R) manufacturing and CMOS technology would allow the production cost of LAE devices to be reduced, and therefore to become affordable to a wider market [31]. Conventional LAE devices are based on either bulk or thin film materials [12, 31, 32]. However, these materials are already obsolete in terms of the requirements of current electronics (lower power consumption, higher efficiency electrical transport, faster switching speeds…), and therefore, novel advanced nanostructured materials, such as inorganic (e.g. semiconductors and metals) and organic materials with the shape of nanowires (NWs) and nanotubes (NTs), have demonstrated an excellent potential as building blocks in many LAE applications, including electronics, optoelectronics, photovoltaics, photonics and sensing [2, 4, 6, 17, 23, 33–44]. The low dimension, long aspect ratio, high crystallinity, high surface-to-volume ratio, high on-currents, high switching speeds, etc. with respect to their counterparts based on bulk or thin film materials, make filamentary nanostructures such as NWs and NTs excellent candidates to improve further the functionality of conventional LAE devices (i.e. based on thin films and bulk materials). Accordingly, organic/inorganic NWs and NTs would allow: 1) fabricating LAE devices on both rigid and flexible substrates [45]; 2) overcoming state-of-the-art planar CMOS technology by scaling on-currents and switching speeds [46]; 3) creating three-dimensional (3D) integrated circuits (ICs) [33]; and 4) continuing the Moore's law due to their higher integrability [47]. However, one of the most important challenges still facing the bottom-up fabrication approach of LAE devices based on nanostructures is the integration and assembly of these nanostructures at well-defined locations over large-area substrates, and with high reproducibility and uniformity. Although many efforts have been expended over recent years, the above drawbacks have not been fully addressed so far.

The fabrication of LAE devices based on nanostructures such as NWs and NTs requires not only high alignment accuracy along the surface of the receiver substrate (e.g. >98% NW directional alignment) [37], but also good

uniformity of the resulting electrical properties (e.g. 10 NWs/μm and 708 NWs/mm^2) [48, 49]. Over the past few years, many efforts have been dedicated to developing high-performance techniques that allow ordered arrays of nanostructures to be deposited on any kind of substrate, including flexible and rigid substrates over large areas. Focusing on the large-area integration of nanostructures on both rigid and flexible substrates, we have compiled the most promising techniques reported in the literature in terms of transfer yield and resulting device performance. Accordingly, we have divided the integration techniques into three main groups, comprising printing, assembly and lithography-based integration techniques as shown in the schematic diagram of Figure 1.1. On the one hand, printing techniques can be separated into two subgroups which depend on the use of either non-contact printing methods (e.g. inkjet printing, aerosol printing, screen-printing…) [50–52] or contact-printing methods (contact-printing, roll-printing, stamp-printing…) [37, 53, 54]. Non-contact printing techniques comprise the use of pastes or inks where nanostructures are conventionally embedded and transferred to a receiver substrate. In these conditions, the nanostructures are not in direct contact with the receiver substrate, and it is the medium (i.e. paste, ink…) that is responsible for the alignment and compactness of the resulting nanostructure layer formed on top of the receiver substrate surface. On the other hand, contact-printing techniques differ between one another in the geometry of the donor and receiver substrates (planar, cylindrical, etc.), and in this case, the transfer

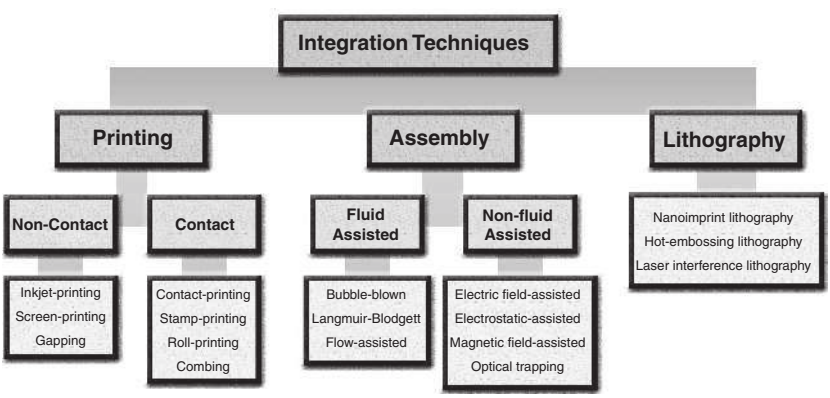

Figure 1.1 Block diagram presenting conventional and novel techniques utilized to integrate micro- and nanostructures over large areas on both rigid and non-conventional flexible substrates.

mechanism comprises the direct contact of the nanostructures with the receiver substrate. The above printing-based techniques have demonstrated their potential and scalability towards large areas – wafer-scale integration of nanostructures – allowing the successful fabrication of LAE devices based on nanostructures and improving nanostructure transfer-yields and process reproducibility. In this regard, printing techniques are a promising near-future approach for nanostructure-based devices, mainly due to their simplicity, low processing temperatures, suitability for large-area and mass production (compatibility with R2R technology), compatibility with two-dimensional (2D) and 3D monolithic integration, reproducibility, reliability and compatibility with flexible substrates. These integration techniques have already demonstrated their validity for developing multi-NW-based LAE devices on both conventional and non-conventional substrates for *e*-skins, integrated circuits (ICs), and high-efficiency interconnectors for the processing of digital information, energy harvesting and storage, consumer electronics, etc. [11, 47].

Assembly techniques mainly use nanostructures in solution, allowing nanostructures to have a 'free' motion in a liquid environment, permitting the use of electric fields (dielectrophoresis or DEP) [55], electromagnetic fields (optical and optoelectronic tweezers) [56], magnetic fields [57], fluidics [58], Langmuir–Blodgett (LB) [59] or bubble-blown (BB) [36] techniques to align – and in some cases to assemble – nanostructures at specific places on the receiver substrate. However, being wet-based, the above techniques present high material wastage and require high-cost and complex systems, hindering their use in the market for commercial applications.

Integration techniques based on lithographic methods, including nanoimprint lithography (NIL) [60, 61], hot-embossing lithography (HEL) [62] and laser interference lithography (LIL) [63] have demonstrated great potential for the development of large-area devices based on micro-/nanostructures not only on conventional rigid substrates but also on flexible non-conventional ones. In addition, the low-cost and rapid fabrication of these techniques make them promising candidates for a wide number of LAE applications based on the nanostructures discussed in this Element [64–67].

This Element shows the state-of-the-art research progress of large-area integration of nanostructures such as organic and inorganic NWs and NTs on both rigid and flexible substrates and their promising functionality in LAE devices. We will discuss the advantages and disadvantages of different integration techniques depending on the properties of the nanostructures, including their compatibility with R2R technology and scalability

over large areas. The Element is organized as follows. Section 2 presents the most relevant organic and inorganic NWs and NTs that conventionally integrate in LAE devices, including common synthesis methods and their most notable properties. Section 3 summarizes printing- and non-printing-based techniques used for the large-area integration of the above nanostructures. Herein, we will emphasize the importance of preserving the properties of as-grown nanostructures during each transfer step, as well as the fabrication of high-quality electrical contacts in LAE devices. Finally, we will conclude by comparing nanostructure-based LAE devices and our future view of coming research avenues for LAE based on novel nanostructures.

2 Nanostructures

2.1 Inorganic Nanostructures

Metal and semiconductor NWs and NTs have been successfully grown from a wide selection of materials, including noble metals (Au, Ag, Cu), metal oxides (ZnO, CuO), nitrides (GaN, Si_3N_4), phosphides (GaP, InP), carbides (SiC), compound semiconductors (InAs, GaAs, CdS) [68–70] and elementary semiconductors (Si and Ge) [71, 72]. For the sake of simplicity, we have classified these nanostructures in two main groups, including metal and semiconductor materials. In this regard, this section will show conventional mechanisms and systems used to synthesize high-crystalline and uniform filamentary inorganic nanostructures with the shape of NWs and NTs, and their most relevant properties and potential applications depending on the material characteristics.

2.1.1 Semiconductor Nanowires

Semiconductor NWs are filamentary nanostructures with high aspect ratio and high surface-to-volume ratio that have been successfully synthesized by bottom-up (Figure 2.1) and top-down (Figure 2.2) approaches [73, 74], depending on their composition and structure, comprising mainly vapour–liquid–solid (VLS) [72, 75–83], vapour–solid (VS) [84], vapour–solid–solid (VSS) [85], solid-liquid-solid (SLS) [86], chemical vapor transport (CVT) [55, 87] and metal-assisted chemical etching (MACE) [17, 88]. The above mechanisms allow semiconductor NWs to be obtained that consist of single elements (Si, Ge) or compounds (III–V, metal oxides, nitrides, phosphides, etc.) with a high degree of control over properties such as crystal quality, aspect ratio, morphology and doping type/level, which are required attributes for high-performance electronics, e.g. electronics,

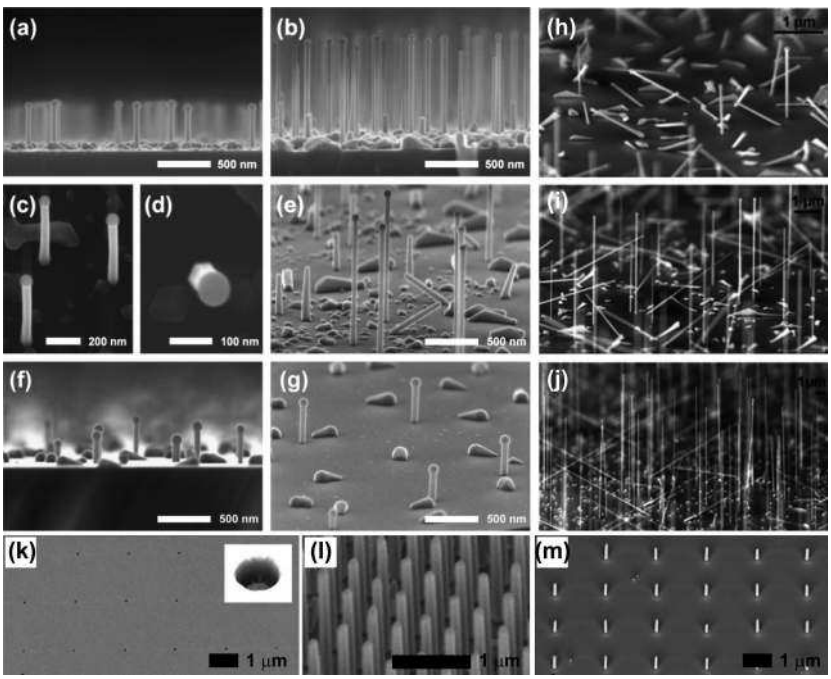

Figure 2.1 (a–g) Scanning electron microscopy (SEM) images of GaAs NWs grown by Ga-assisted VLS synthesis procedure in CBE system. Reprinted with permission from García Núñez et al.[77] Copyright © 2013, Elsevier B.V. (h–j) SEM images of GaAs NWs grown by Ga-assisted VLS on pre-patterned substrates. Reprinted with permission from Russo-Averchi et al.[115] Copyright © 2012, Royal Society of Chemistry. (k–m) SEM images of InAs NWs grown by selective area epitaxy (SAE). Reprinted with permission from Hertenberger et al. Copyright © 2010, AIP Publishing.

sensors and photovoltaics [24, 41], UV photodetectors [55, 84, 89–91], high mobility FETs [2, 6], flexible electronics [4, 6], multifunctional electronics [33] and single electron-based transistors [92].

The most extended and successful systems used to carry out the synthesis of semiconductor NWs through the aforementioned approaches are chemical vapour deposition (CVD) [93], laser ablation cluster formation [83], metal-organic chemical vapour deposition (MOCVD) [73], molecular beam epitaxy (MBE) [75, 76, 78] and chemical beam epitaxy (CBE) [77, 94]. In addition to a pure phase NW [77], the above techniques have demonstrated tremendous potential for carrying out nanoengineering along with the NW structure, morphology and composition, enabling e.g. the fabrication of

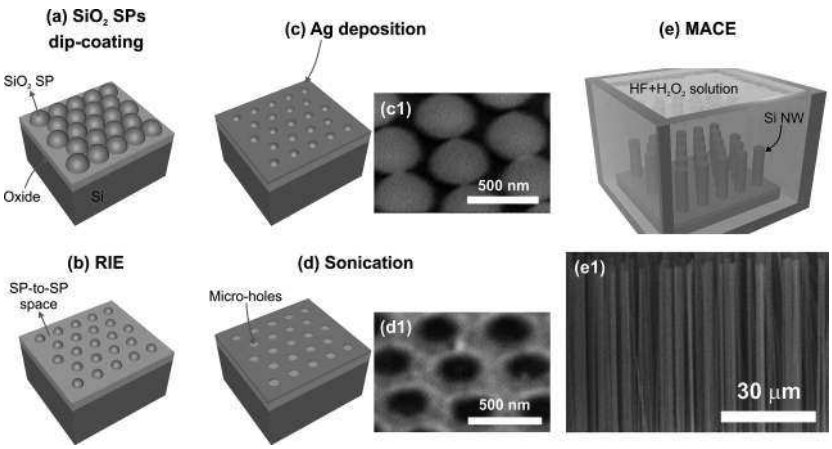

Figure 2.2 3D schema of top-down approach, namely MACE, showing experimental steps for the synthesis of Si NWs, comprising: (a) dip-coating of SiO_2 micro-spheres (SPs) over a large-area Si wafer surface; (b) reactive-ion etching (RIE) of SiO_2 SPs; (c) deposition of 100–200 nm of Ag layer (see the SEM image in [c1]); (d) sonication in isopropanol for 5 min creating a periodic metal nanomesh (see the SEM image in [d1]); (e) MACE process dipping the sample in a HF/H_2O_2 solution for 30 min, resulting in vertically aligned Si NWs (see the SEM image in [e1]). Reprinted with permission from García Núñez et al.[17] Copyright © 2018, American Chemical Society.

core–shell structures [95], superlattices [96] and polytypic and twinned structures [97].

One of the key aspects of successful LAE device manufacturing based on nanostructures is the current possibility to synthesize high crystal quality NWs over large areas. For example, in either top-down [17] or bottom-up approaches [77], the use of metal and dielectric nanoparticles over large areas for VLS (Figure 2.1) and MACE synthesis (Figure 2.2), respectively, have allowed the synthesis e.g. of III–V NWs (Figure 2.1[a–g]) [77, 98], metal oxide NWs [55, 84, 99, 100] and IV NWs (Figure 2.1[h,i] [72], Figure 2.2[e1] [17]) at wafer scale.

Group III–V Semiconductor Nanowires

The growth of III–V semiconductor compounds with the shape of NWs has been successfully demonstrated for arsenides (III-As) [98, 101], phosphides (III-P) [102, 103], nitrides (III-N) [104, 105] and, more rarely, for antimonides

(III-Sb) [106]. The possibility to grow these semiconductor materials makes this kind of NWs attractive for the development of many applications, including electronics, optoelectronics, photonics, photovoltaics, sensing, etc. [107–109]. III–V semiconductor NWs are conventionally grown in CBE, MBE and MOCVD systems by the well-known metal-assisted VLS mechanisms [110]. Au is typically used as the metallic catalyst to guide the growth of the NWs, mainly due to the possibility of forming an eutectic with most of the III–V elements involved in the NW growth [111]. For that, Au nanoparticles (NPs) are typically formed on top of the growth substrate mainly through two different strategies, involving: i) spin-coating (or drop-casting) of Au colloidal NPs covering the surface of the growth substrate [112], or ii) de-wetting of Au thin films to produce Au NPs [113]. Alternatively, III–V NWs have also been grown by processes such as self-catalysed VLS, comprising the use of the element III (i.e. Ga, In, etc.) as the catalyst of the VLS growth. For example, the Ga-assisted VLS growth of high crystal quality GaAs NWs with pure zinc blende structure has been demonstrated (Figure 2.1[a–g]) [78, 81]. Self-assisted methods prevent the use of foreign materials such as Au, which can hinder or affect the resulting electronic and optoelectronic properties of the NW due to the intentional incorporation of Au into the III–V structure [114]. The advances demonstrated in lithography techniques that allow the definition of metallic NPs with great control over features such as NP size, NP position, NP-to-NP spacing, NPs density, etc. have fostered the scaling of III–V NW growth towards wafer scales [115]. The utilization of pre-patterned growth substrates, typically consisting of Si(111) substrates covered by a thick layer of SiOx and nano-holes predefined along its surface, has made Ga-assisted growths a promising method to achieve the large-area growth of III–V NWs (Figure 2.1[h–j]) [115].

On the other hand, III–V NWs have also been grown by catalyst-free processes [116]. The above advances in high-performance lithography methods permit great control over the dimensions of the NW (diameter and length), limiting the growth of the NW at specific locations distributed along the growth substrate surface (Figure 2.1[k–m]). Typically, nanometric holes are defined by electron beam lithography on thick oxide layers, which inhibits the nucleation of III–V on the oxide while promoting the preferential nucleation of III–V only in the defined nanopores (Figure 2.1[j]). This technique – namely, selective area epitaxy (SAE) – is one of the most promising approaches for the growth of III–V NWs at wafer scale, and therefore attractive for the development of LAE. The absence of any catalyst in the growth process is considered a key advantage of the method, preventing the formation of unintentional defects along the NW structure and therefore improving the quality of the resulting NW through a

pure phase crystal. The high level of control over the position and density of NWs over the growth substrate is also considered one of the most compatible features with the techniques described in Section 3 for the development of LAE. The possibility of growing free-standing NWs with a tuneable NW footprint dimension and specific location (Figure 2.1[k,l]), increases the applicability of as-grown NWs to a wider number of circuit layouts.

Group IV Semiconductor Nanowires

IV group semiconductors stand out over the other semiconductor materials, because of their compatibility with both bottom-up [110] and top-down synthesis approaches [17, 88]. Although III–V and metal oxide semiconductors have been grown by top-down methods [117], the crystal quality of the resulting NWs is still far from the results reported for IV group NWs (Figure 2.2[e1]) [17]. The great compatibility of IV group NWs with top-down synthesis approaches is based on the mechanism governing the synthesis process. In MACE, the NWs are synthesized from the wafer, which makes this process scalable towards wafer level fabrication of free-standing NWs. In this scenario, the NWs take the crystal structure, doping level and preferential orientation of the original wafer. For example, the MACE synthesis of Si NWs demonstrates the possibility of growing Si(100) NWs vertically aligned on a Si(100) substrate through the steps described in Figure 2.2(e1). One interesting approach that allows the MACE synthesis over large areas comprises the use of metallic nanomesh to mask specific areas of the substrate, exposing the rest to the etching solution. For example, SiO_2 colloidal NPs have been dip-coated on the surface of a Si(100) substrate (Figure 2.2[a]) to create a nanometallic mesh that was used as a catalyst in MACE synthesis of Si NWs (Figure 2.2[b–d]) [17]. In this scenario, the pore size (Figure 2.2[d1]) can be roughly controlled by the initial size of the SPs. The fundamental principle of MACE consists in the use of an etching solution (e.g. HF/H_2O_2 for Si wafers) promoting the preferential etching of the Si wafer underneath the Ag layer (Figure 2.2[e]) and resulting in vertically aligned Si NWs on top of the Si wafer (Figure 2.2[e1]). Therefore, this is a promising low-cost and easy-to-develop approach for improving the quality of NW samples for their integration over large areas through the techniques explained in Section 3.

Group IV semiconductor NWs have also been synthesized successfully by bottom-up approaches such as Au-assisted VLS. Indeed, as stated previously, VLS theory was firstly proposed to explain the growth of Si NWs on Si substrates using Au nano seed as catalyst (Figure 2.3[a]) [118]. After its first statement, Au-assisted VLS has been further researched, demonstrating the

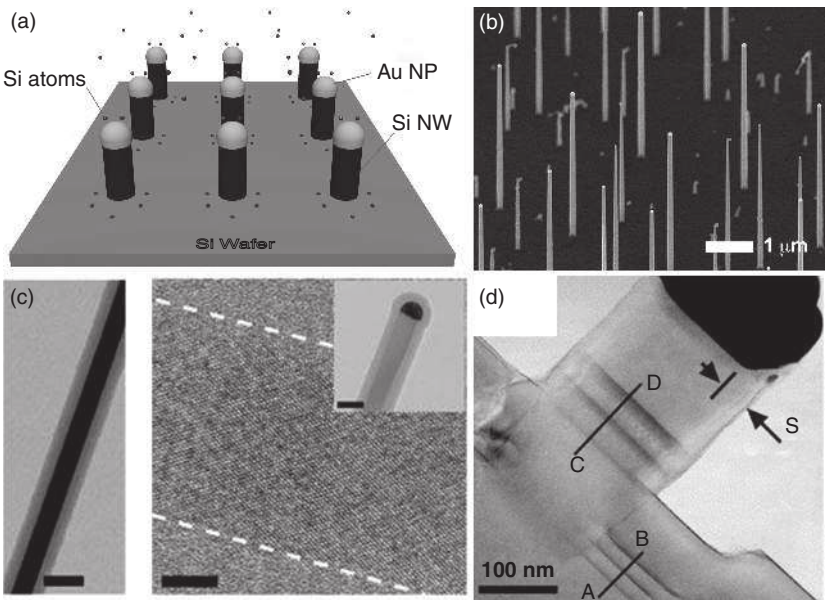

Figure 2.3 (a) 3D schema and (b) SEM image of Au-assisted VLS Si NWs. Reprinted with permission from Hannon et al. [72] Copyright © 2006, Springer Nature. (c) SEM image of i-Si/SiO_x/p-Si core–shell NWs. Reprinted with permission from Lauhon et al. [120] Copyright © 2002, Springer Nature. (d) Transmission electron microscopy (TEM) image of Si/Ge longitudinal heterostructures grown along a Si NW by VLS. Reprinted with permission from Zakharov et al. [122] Copyright © 2006, Elsevier B.V.

growth of longer free-standing NWs made of Si (Figure 2.3[b]) [72], Ge [71, 119], and even the fabrication of heterostructures based on these materials, including Ge/Si, i-Si/SiO_x/p-Si, i-Si/p-Si core/shell structures (Figure 2.3[e]) [120, 121] and longitudinal heterostructures (Figure 2.3[d]) [122] with the shape of a NW.

Metal Oxide Semiconductor Nanowires

Among all metal oxide materials that can be synthesized with the shape of a NW, ZnO is one of the most attractive metal oxide nanomaterials for the development of LAE. The growth and characterization of ZnO NWs have been thoroughly studied during decades, and therefore, extensively reported in the literature [123–126]. Due to their facile fabrication procedure and excellent properties (high surface-to-volume ratio, high surface reactivity,

wide band gap, sensitivity to UV light, piezoelectric effects, biocompatibility, etc.), ZnO NWs have been considered a great candidate for the development of a wide range of applications, including sensors (gas sensors [127], photodetectors [55], and chemical sensors [128]), photovoltaic cells [129], photonics [130], energy harvesters (piezoelectric nanogenerators [131], and triboelectric nanogenerators [132]) and energy storage devices (supercapacitors, and batteries) [133]. These investigations have been fostered thanks to the advances achieved in the synthesis of ZnO NWs. Accordingly, the growth of ZnO NWs have been successfully demonstrated by using various methods, which can be mainly classified in two different groups depending on the growth temperature. High temperature growths (i.e. 500–1500 °C) are usually carried out in gaseous environments in closed chambers such as physical vapour deposition (PVD) [134], CVD [135], MBE [136], pulsed laser deposition (PLD) [137] and high-temperature furnace through chemical vapour transport (CVT) (Figure 2.4[a–c]) [55, 84, 99, 100]. Alternatively, ZnO NWs have been grown by low temperature methods (< 200˚C), comprising the use of solution environments. Solution-based growths mainly include hydrothermal methods [138–140] and electrochemical deposition [141].

Under high temperature growth conditions, ZnO NWs have been successfully grown mainly by VLS and VS mechanisms [55, 84, 87]. Although it has been rarely reported, ZnO-seeded VS growth of ZnO NWs have been demonstrated [87]. In VLS conditions, there are two accepted models – namely Gibbs–Thomson and the diffusion model – that explain the relation between length and diameter of the resulting NWs. One can clearly identify that ZnO NWs are growing through the Gibbs–Thomson model if the characterization of the resulting NWs presents an increase in the NW length when the diameter of the NW increases [142]. In this scenario, the adatoms are directly attached to the NW tip (solid phase) after diffusing through the liquid metal catalyst located at the tip of the NW. In contrast, when the growth of the NW is governed by the diffusion model, the NW growth is limited by the diffusion of adatoms along the NW sidewalls, resulting in NW lengths inversely proportional to the NW diameter [143].

In metal-assisted VLS of ZnO NWs, governed either by Gibbs–Thomson or diffusion model, Au nanoparticles are typically used as catalyst (Figure 2.4[c]), acting as a trap for growth species, i.e. Zn and O_2 gases. The supersaturation of the Au catalyst produces a precipitation of ZnO crystals to the interface formed between the catalyst and the substrate surface. ZnO crystals nucleate under the catalyst and on the substrate