Rapid Thermal and Integrated Processing VII

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Rapid Thermal and Integrated Processing VII

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PREFACE

The 1998 MRS Spring Meeting symposium on "Rapid Thermal and Integrated Processing" was one of the most exciting meetings in recent years. The papers presented at this symposium illustrate how the range of rapid thermal processing (RTP) applications in silicon device manufacturing is rapidly expanding, and how mature the technology has become.

The first day of the symposium covered modelling of RTP equipment and techniques for temperature measurement and control. Many characteristics of RTP technology arise from the impact of the optical properties of semiconductor wafers on thermal response and on pyrometric temperature measurement. Papers covering equipment issues illustrate that problems such as temperature uniformity and measurement, traditionally viewed as limitations for RTP technology, are well on the way to being resolved.

Perhaps one of the most exciting and dynamic areas of RTP research is in the field of gate dielectrics, where RTP offers a variety of paths for the creation of the very thin films. Future MOSFETs with channel lengths less than 0.1 µm will require an equivalent oxide thickness of 15Å or less. At this thickness, SiO_2 ceases to be a viable material because of carrier tunneling, which results in gate leakage. This technological barrier was one of the key themes to emerge from the symposium. Several papers showed that RTP can provide unique capabilities for dielectric formation. Papers covered a large spectrum of solutions ranging from the use of nitrogen-doped oxides to new high-dielectric constant materials. A panel discussion was also held on ultrathin gate dielectrics, which attracted a large audience. The panelists were M. Green (Lucent Technologies), J. Kuehne (Texas Instruments), B. Triplett (Intel), J. Hauser (North Carolina State University), and D.L. Kwong (University of Texas at Austin). The discussion suggested that silicon nitride could provide an important stepping-stone on the path to more radical alternatives based on high-dielectric constant materials.

The symposium also included sessions covering the other vital ingredients for advanced MOSFET engineering, such as alternative gate electrode materials and new RTP processes for ultrashallow source/drain junctions and low-resistivity silicide contacts. Several papers showed how optimized integration of SALICIDE and source/drain process modules can lead to significant improvements in electrical device characteristics. The formation of shallow junctions by the combination of low-energy ion implantation and RTP anneal continues to be an important process for advanced devices. In this arena, the effects of transient- and oxidation-enhanced diffusion on junction depth were the focus of several papers, which analyzed the impact of the heating rate during anneal and the composition of the gas ambient. Gas purity also emerged as a key parameter in formation of advanced silicides. Rapid thermal chemical vapor deposition (RTCVD) techniques were also presented with a range of applications in the formation of MOSFET channels, ultrashallow junctions and their contacts. Novel RTCVD techniques were also considered for forming advanced MOSFETs including vertical structures.

The symposium ended with a session on new applications of RTP, which included processes outside silicon processing where RTP allows the creation of structures inaccessible through conventional thermal processing.

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July 1998

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S. Radelaar
B. Peuse
M.L. Green
J.R. Hauser
E.J.H. Collart
W. Lerch
J.C. Sturm
K. Maex
R. Singh

who graciously accepted to share their expertise in their respective fields with other attendees of the symposium. Their contributions added immensely to the success of our meeting.

We sincerely express our gratitude to our panelists:

B. Triplett
J. Kuehne
M.L. Green
J.R. Hauser
D.L. Kwong

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