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Materials, Technology and Reliability for Advanced Interconnects and Low-k Dielectrics

Editors: G. S. Oehrlein, K. Maex, Y. -C. Joo, S. Ogawa and J. T. Wetzel

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**Materials, Technology and
Reliability for Advanced
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Materials, Technology and Reliability for Advanced Interconnects and Low-k Dielectrics

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PREFACE

These proceedings are a record of Symposium D, "Materials, Technology and Reliability for Advanced Interconnects and Low-k Dielectrics," held April 23–27 at the 2000 MRS Spring Meeting in San Francisco, California, and highlight important achievements and challenges in advanced interconnects and low-k dielectrics as employed in the microelectronics industry. The replacement of Al alloys with Cu along with the introduction of new barrier materials to protect Cu from chemical attack, and the utilization of new dielectric materials with a lower relative dielectric constant k than SiO_2 in multi-level metallization structures of increasing complexity, are the major themes of evolution in this field. Invited reviews illustrate the significant progress that has been achieved, and they pointed out the challenges. Contributed papers presented by researchers from different countries demonstrated progress on current topics using a truly multidisciplinary approach. A few brief comments on each topic that will be dealt with in more detail in reviews and papers are presented here as an introduction to these Proceedings.

Interconnects must be reliable from mechanical, chemical and electrical points of view. Mechanical properties of multilevel metallization structures are addressed by examining the mechanical strength of the primary materials themselves and the properties of composite structures. Of particular interest are the mechanical properties of a variety of novel low-k materials and the adhesion between metal/dielectric films, fracture and delamination mechanisms. Liner or barrier layers on metal and dielectric surfaces or interfaces are employed to protect the metals and dielectrics from the chemical attack of impurities and prevent chemical interactions. New diagnostic approaches are required to characterize locally the variation of the mechanical properties at dielectric/barrier and barrier/metal interfaces. Characterization and control of the electromigration and stress migration characteristics of multilevel structures is basic to producing reliable interconnects.

The introduction of a true low-k dielectric material for use as the inter- and intra-line insulator promises the most significant reduction of RC-delays since the introduction of Cu. The widespread use of such a material has been slow because of the significant changes in process flows that is required, materials reliability concerns, and a marginal reduction of the dielectric constant for many of the alternative dielectric materials that have been considered. Process integration and compatibility of current low-k materials with conventional fabrication sequences is a significant issue. Nano-porous low-k materials are possibly the most important candidates that will satisfy the spectrum of technological requirements in the long-term.

The deposition of barrier and/or seed layers with satisfactory properties is a prerequisite of successful metallization. This demands the investigation of novel deposition techniques that provide sufficient control of deposited film properties, and the verification of the properties of the deposited films by a set of complementary measurement techniques. The characterization of deposited metal film properties, the evolution of surface texture and grains, either during synthesis or in post-processing, and the performance and reliability of the interconnects is also of central interest, especially for Cu. Satisfactory post-processing of deposited Cu films and barrier layers, in particular chemical mechanical planarization to define the Cu lines, is an important challenge that has to be overcome for manufacturable advanced multilevel metallization structures.

G.S. Oehrlein
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