Applications

BURIED OXIDE CHANNEL FIELD EFFECT TRANSISTOR

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ABSTRACT

A room temperature oxide channel field effect transistor with the channel on the surface was recently demonstrated at IBM which showed switching characteristics similar to conventional silicon FETs. In this paper we introduce a new architecture for the oxide channel transistor where the oxide channel material is buried below the gate oxide layer. This buried channel architecture has several significant advantages over the surface channel design in coupling capacitance, channel mobility, and channel stability. We will discuss the design and fabrication of the buried channel oxide FET and we will present results from these devices which demonstrate a higher transconductance.

INTRODUCTION

The drive toward higher density semiconductor integrated circuits has been fueled for decades by the scalability of silicon MOSFET technology. Unfortunately there are fundamental physical effects which might limit the scaling of this technology beyond 30 nm.[1] Driven by the search for a potentially scalable technology, a novel field effect transistor (FET) has recently been proposed [2-5] which utilizes a material capable of undergoing the Mott metal-insulator transition [6-8] as the channel material. Such an FET is similar to a conventional silicon MOSFET in that there are source and drain electrodes on either end of a channel and a gate oxide and gate electrode which produce a field terminating in the channel. The channel, however, consists of a material capable of undergoing the Mott metal-insulator transition rather than a semiconductor. A Mott insulator is a material in which the electrons are localized as a result of the Coulomb interaction between electrons rather than due to the ionic potential as in most insulators. In our devices the transition between insulating and metallic states of the channel is induced by the gate field leading to strong switching characteristics. One promising class of oxide materials for the channel is the cuprate family of perovskite structure materials related to high temperature superconductors. Due to the widespread interest in high temperature superconductivity the cuprates have been extensively characterized and a substantial materials knowledge base exists for these materials. One of the challenges of such devices is that the surface charge density the gate field must produce is estimated [2,3] to be ~10^{14} carriers/cm^2, requiring the use of gate oxides with high dielectric constant and high breakdown field. Again the cuprates are attractive since they offer epitaxial compatibility with gate materials such as strontium titatate (STO) and barium strontium titanate (BST) which have been demonstrated to have a high dielectric constant and high dielectric breakdown field [9-11] capable of producing the required surface charge density. Despite the challenges, a buried oxide-channel field effect transistor (OxFET) is of interest because of the potential to scale such a device beyond the silicon scaling limits due to the absence of impurity doping in these materials and since the charge separation layer at the source and drain contacts is expected to be on the ~1 Angstrom scale rather than ~100 Angstrom.[3]

We would like to make an important distinction. At first glance, the structures we fabricate resemble those of the superconducting FET structures proposed and built by several

Mat. Res. Soc. Symp. Proc. Vol. 623 © 2000 Materials Research Society

groups [12-15]. The structures are almost identical in most cases, however, the details differ as do the experimental conditions and the goals. The most important contrast is that all the data shown in this paper and in references [2,4,5] are obtained in *room temperature* operation. In the superconducting FET proposals, the goal was to induce (or inhibit) superconductivity in a channel by modulating the carrier concentration with a gate potential. Our work concentrates exclusively on the normal state properties of the cuprate films.

DEVICE ARCHITECTURE

An OxFET with the channel material on the surface of the device was recently demonstrated at IBM in which the channel material was $Y_{1-x}Pr_xBa_2Cu_3O_{7-\delta}$ (YPBCO).[2] The devices which were demonstrated had a simple architecture illustrated in figure 1 which was chosen for ease of fabrication. In this structure all the materials fabrication is done via pulsed laser deposition (PLD) directly on an unpatterned substrate and the source and drain contacts are directly deposited on the films through a stencil mask. The substrate in this case is niobium doped strontium titanate (Nb:STO) which is a conducting material. The substrate therefore also acted as the gate electrode. The gate dielectric (STO) is deposited on the substrate first, and then the channel material (YPBCO) was deposited. The surface channel FET had characteristic curves similar to conventional silicon MOSFET curves with a transconductance of ~ 2 μS at a drain voltage of 1 volt and a gate voltage of 10 volts. ON/OFF ratios of up to 10^4 were observed. However, despite the ease of fabrication of the surface channel devices there are several disadvantages to the surface channel architecture.

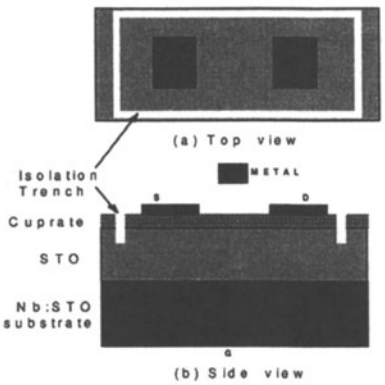

Figure 1: Surface channel architecture (a) top view (b) side view.

In the surface channel devices, the substrate also serves as the gate electrode. Therefore, there is a very large capacitance associated with the gate and there is a strong coupling capacitance to other devices. This makes operation at high frequencies impossible. Another significant disadvantage of the surface channel architecture is a result of moisture sensitivity of the cuprate materials as a class. Since the cuprate is an unshielded top layer, it slowly deteriorates due to water contamination, making necessary the deposition of thick cuprate films to protect the switching layer near the gate oxide/channel interface. However, the source and drain electrodes are only in direct contact with the upper (unswitched) part of the cuprate film. Thus the surface

channel architecture has two limiting problems: First, there is a potential resistance (in series with the channel) which could limit the "ON" state performance of the device due to conduction through unswitched cuprate layers from the source and drain electrodes to the switched part of the cuprate channel near the gate oxide/channel interface. Second, there is a potential resistance (in parallel with the channel) which could limit the "OFF" state performance of the device due to conduction from the source to the drain through the unswitched part of the cuprate channel. Due to the short electric field screening length in cuprate channels in the conducting state, OxFET devices are strongly dependent upon the quality of the cuprate near the gate oxide/channel interface. This is because only the cuprate within an electric field screening length of the gate oxide/channel interface is switched. Of course, long-range order is paramount to the best transport in any material. This is particularly true in our devices due to the interface nature of the switching. Any grain boundaries in the interfacial film will degrade the mobility of the devices. Therefore it is important to make the highest quality interface. Although the substrates we start with are atomically smooth, in the surface channel devices, the cuprate is deposited only after the gate oxide is deposited. After depositing a ~1000 Angstrom gate oxide film on the atomically smooth substrate, the cuprate interface might not be as smooth as would be the case if the cuprate were deposited first.

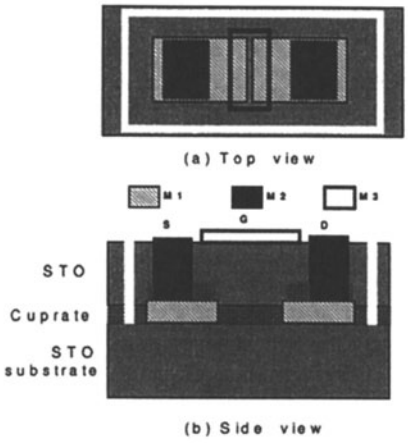

Figure 2 : Buried channel device architecture (a) top view (b) side view.

The buried channel OxFET architecture provides a solution to several of these limitations although the fabrication is now more complicated. The buried channel OxFET architecture is shown in Fig. 2a (top view) and 2b (side view). The substrate is nonconducting undoped strontium titanate (STO) and the gates are now independent for each device since they are deposited on the top of the structure through a lithographic process. The cuprate channel is now directly on the atomically smooth substrate ensuring the highest quality interface. The cuprate channel is also protected from moisture by the gate oxide layer. The source and drain electrodes make direct contact with the cuprate material at the gate oxide/channel interface eliminating the potential series resistance. Since the cuprate is protected from moisture by the gate oxide layer, the cuprate channel layer can eventually be made thinner thereby reducing the potential parallel

resistance. Also, since the substrate is insulating the large gate capacitance and coupling capacitance to other devices is eliminated.

FABRICATION

Fabrication of the devices starts by putting the first metallization layer (M1) on the undoped STO substrate. This is accomplished using standard lithographic techniques. The M1 metallization is critical since it defines the channel geometry. Since the M1 process involves a lithographic step and a liftoff step, we were concerned about the quality of the STO surface after M1 processing. AFM measurements showed that the STO surface in the channel between the source and drain M1 electrodes remained atomically flat. Further, ion scattering studies [16] have shown that the initially Ti terminated Kawasaki [17] processed STO substrate is left with a Sr rich surface after liftoff, oxygen ashing, and cleaning. This is fortuitous since a Sr terminated surface is better in preventing copper oxide precipitation [18] during the pulsed laser deposition of the cuprate channel. After M1 metallization, liftoff, oxygen ashing, and cleaning, the substrate with M1 is placed in a PLD chamber for thin film deposition. The cuprate film used for these experiments was La_2CuO_4 (LCO). The LCO was grown at a temperature of 700 C in an oxygen background pressure of 10 mTorr. The LCO film thickness was approximately 100 Angstrom. Immediately after the LCO growth, a 1000 Angstrom film of STO was grown on top the cuprate. The oxygen pressure was 250 mTorr and the temperature was 760 C for the STO film growth. After deposition, the films were slowly cooled to room temperature in 1 atm of oxygen. After film deposition, processing continued with lithographic definition of M2 vias to make contact with the buried M1 metallization. A combination of chemical etching and ion milling was used to make vias down to the M1 metallization. The vias were then metallized and M2 was defined in the liftoff. Next, the M3 metallization, which defines the gate electrodes, was accomplished with another lithographic step, metallization, and liftoff. Finally, the devices were isolated from each other by making a trench around each device down to the STO substrate. This was done using lithographic techniques to define the trenches and ion milling and chemical etching to make the trenches.

RESULTS

The completed devices were tested using a Hewlett-Packard 4145 semiconductor parameter analyzer with a grounded source electrode. In Fig. 3 we plot the drain current (I_d) versus gate voltage (V_g) for a constant drain voltage of 1 volt. In Fig. 4 we plot the transconductance (dI_d/dV_g) versus gate voltage. The devices show a transconductance of up to 45 μS at 1 volt drain voltage and a gate voltage of 2 volts for a channel length of 1 μm and width = 150 μm. This is an improvement over the transconductances seen in the surface channel devices. We expect that the better interface quality of the buried channel devices leads to a higher mobility and therefore a higher transconductance. One limitation of the buried channel devices is that the "OFF" state conductance is still high in these devices. The maximum $\Delta R/R$ we observed was 240%. However, we have not yet optimized the process for "OFF" state conductance. This is most likely the result of a parallel conduction channel associated with the unswitched layers in the films that we have made so far.

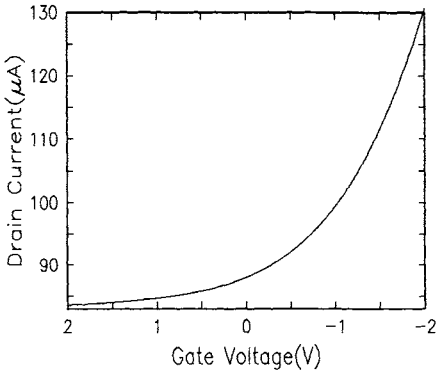

Figure 3: Drain current versus gate voltage for a buried channel architecture device.

An interesting observation is the gate field dependent mobility. This is illustrated in Fig. 4. Since transconductance is proportional to mobility, this curve suggests a linear increase in mobility with gate field above threshold. This is consistent with a picture of a mobility transition in these materials in going from the insulating state to the metallic state.

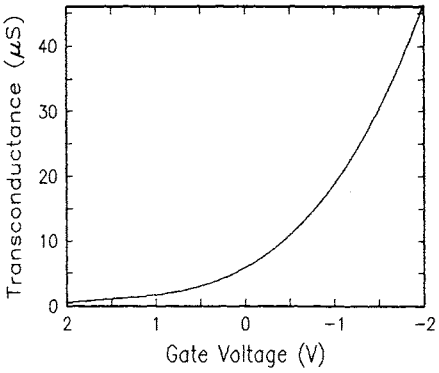

Figure 4: Transconductance versus gate voltage for a buried channel architecture device.

The Mott metal-insulator transition induced by electric field is expected to occur at a surface charge density of 10^{14} carriers/cm^2 [3]. In order to determine whether the present gate oxide films are achieving the theoretical transition charge density we have measured the capacitance of our devices as a function of voltage. The surface charge density is limited by two factors, the dielectric constant for the film and the breakdown potential for the film. Although the bulk dielectric constant for STO is ~300 [17], the value usually decreases in thin films. The dielectric constant we determine for our film (thickness = 1000 Angstrom) is 180. Further, the

dielectric constant decreases with voltage. The breakdown potential for the tested film was 8 volts. Thus we find that the maximum surface charge density we attain in the present films is < 0.5 x 10^{14} carriers/cm^2. This indicates that more work needs to be done with the gate dielectric to optimize the surface charge density. Processing improvements might be made to improve the quality of films of the current thickness. For example, in RF sputtered STO thin films it was found that a dielectric constant higher than the bulk value can be attained under proper conditions [19]. In addition, detailed studies of the dielectric constant and the breakdown potential versus film thickness are necessary to find the optimal film thickness.

SUMMARY

We have demonstrated devices of a buried channel architecture for room temperature oxide field effect transistors with a channel capable of undergoing the Mott metal-insulator transition. This architecture utilizes a buried interface for the gate oxide/cuprate channel to improve the quality of the interface, protect the cuprate from moisture, reduce contact resistance to the channel, and reduce gate capacitance and coupling capacitance to other devices. An improvement in transconductance of these devices expected from the better mobility of a higher quality gate oxide/channel interface was observed.

ACKNOWLEDGEMENTS

The authors gratefully wish to acknowledge many stimulating discussions with B.A. Scott, D.M. Newns, C.C. Tsuei, and A. Gupta.

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