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Silicon Materials—Processing, Characterization and Reliability

Editors: Janice L. Veteran, David L. O'Meara, Veena Misra and Paul S. Ho

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Silicon Materials—Processing, Characterization and Reliability

Editors: Janice L. Veteran, David L. O'Meara, Veena Misra and Paul S. Ho

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PREFACE

This volume contains papers presented at Symposium B, "Silicon Materials—Processing, Characterization and Reliability", held April 1-5, at the 2002 MRS Spring Meeting in San Francisco, California. The symposium was designed to address all aspects of silicon processing, exclusive of junction formation, which was covered in Symposium C. The breadth of the symposium provided a forum to select a larger percentage of high-quality reports in each technically critical area, such as: high-k dielectrics, gate array designs, metal gates, copper interconnects, and low-k dielectrics. The technology reviewed included research, development and manufacturing aspects. Over 220 papers were presented, however, only 102 papers were submitted for publication.

A half-day tutorial on silicon processing kicked off the symposium on Monday morning. The tutorial, presented by Earnest Levine, covered both the technical side of processing as well as the realities of the manufacturing environment. The tutorial was well attended.

The tutorial was followed by four and one-half days of oral presentations, and three evenings of poster presentations. This symposium was one of the largest at the 2002 MRS Spring Meeting.

In the first session, metrology techniques and silicon-on-insulator issues were presented. The second, third and fourth sessions addressed issues with high-k dielectrics for use as gate insulators. The fifth, sixth and seventh sessions primarily focused on interconnect issues, low-k dielectrics, and device modeling. Sessions eight, nine and ten continued with additional papers on interconnects and low-k dielectrics, including a joint session with Symposium C with an invited talk on SIMS analysis techniques. Back-end techniques, analytical techniques, and reliability issues were discussed in sessions eleven, twelve and thirteen. An excellent invited talk was given in session twelve on new methodologies for finding defects in complex circuitry.

In general, the presentations and papers provide a glimpse into the technical status of the semiconductor industry. The evolution of transistors to miniaturization beyond the capabilities of conventional IC processing has created a need for materials research in many levels of the integrated circuit fabrication, including new materials in substrates, gates and interconnects. The transition from silicon-based chemistries to alternative materials makes one appreciate the unique properties of silicon that have permitted the dramatic progress in semiconductor device advancement in the past. New materials and techniques to process and evaluate the materials will continue to be required to extend the device advancements, with the continual constraint of commercial viability.

The symposium organizers wish to thank the session chairs and the student assistants, who helped ensure an excellent symposium by assisting in the timely and smooth execution of the technical papers. We also wish to thank all of the authors for their presentations at the symposium and their contributions to these proceedings.

Finally, we wish to thank and acknowledge the financial support for this symposium, which was provided by Applied Materials, Tokyo Electron America, Inorgtech, Ltd., and MMR Technologies, Inc.

Janice L. Veteran
David L. O'Meara
Veena Misra
Paul S. Ho

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