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Suppression of Parasitic BJT Action in Single Pocket Thin Film Deep Sub-Micron SOI MOSFETs.

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ABSTRACT

A study of parasitic bipolar junction transistor effects in single pocket thin film silicon-on-insulators (SOI) nMOSFETs has been carried out. Characterization and simulation results show that parasitic bipolar junction transistor action is reduced in single pocket SOI MOSFETs in comparison to homogeneously doped conventional SOI MOSFETs. A novel Gate-Induced-Drain-Leakage (GIDL) current technique was used to characterize the SOI MOSFETs. 2 - D simulations were carried out to analyze the reduced parasitic bipolar junction effect in single pocket thin film SOI MOSFETs.

INTRODUCTION

The advantages of SOI MOSFETs over their bulk counterparts are: simple dielectric isolation, increased circuit speed, elimination of latch up, reduced short channel effects and lower Hot Carrier Effects (HCE) [1]. The SOI technology has also shown great potential for mixed mode and analog applications [2]. However, the presence of buried oxide beneath the silicon film leads to floating body effects [3]. These floating body effects are detrimental to the operation of MOSFETs particularly in mixed mode/analog applications. The high drain field in deep sub-micron devices causes the impact ionization. The electrons move towards the drain, whereas holes move towards the film body region where they get accumulated. The floating body effect can give rise to kink and parasitic bipolar junction transistor (pBJT) action. The kink should be avoided but is not harmful in digital operation. The pBJT effect is detrimental especially in mixed mode analog/digital applications. Hence it needs to be constrained. Thin film SOI MOSFETs do not show the kink, but their circuit performance is severely restricted by the pBJT effect. In long channel devices, the holes recombine before reaching the source, whereas in short channel devices the hole current gets amplified by the BJT gain β, which depends on the base width (channel length). This amplified current gets added to the drain current. The major problems due to lateral bipolar gain are the parasitic BJT induced latch-up [4] and lowering of breakdown voltage [5].

Channel engineering has been successfully used to overcome some of the undesired effects in the MOSFET's. Symmetric halo implantations are widely used in the bulk technology for the improvement of Short Channel Effects (SCE) and HCE [6]. Recently, asymmetric channel implantation at the source end has been introduced for bulk [7,8] MOSFETs. These Single Pocket (SP) devices show an improvement in the device performance like reduction in Drain Induced Barrier Lowering (DIBL) and threshold voltage (V_{th}) roll-off. The advantages of bulk asymmetric device for mixed mode applications have also been recently reported [9]. The SP implantation has also been introduced in the SOI technology [10]. In this work we have analyzed the parasitic bipolar junction transistor effect of SP thin film nMOSFET's and have

shown that these devices have less parasitic bipolar gain compared to the Conventional (CON) homogenously doped SOI MOSFET's.

Parasitic bipolar gain β of the MOSFET was experimentally characterized by the Gate Induced Drain Leakage (GIDL) current technique in both CON and SP SOI MOSFETs. The suppression of parasitic BJT effect in SP SOI devices is also analyzed from 2-D simulations and is attributed to a lower peak electric field near the drain junction. Detailed process and device simulations using a BJT like structure with similar technology parameters as in SP-SOI provided further insight. The results obtained from simulations qualitatively corroborate the experimental findings.

DEVICE FABRICATION

SOI MOSFETs used in this study were fabricated by a standard CMOS process, except for the threshold voltage implant, which is done after the poly-silicon gate patterning for SP devices using a tilt implant from the source side. Poly-silicon gate was defined by electron- beam lithography. Pocket implant is done from the source side at a tilt angle of 15°. Both the CON and SP SOI MOSFETs were fabricated on the same wafer with channel lengths down to 100 nm in the same process. The silicon film thickness (T_{SOI}) is 50 nm and the buried oxide thickness is 180 nm. The gate oxide thickness for all the MOSFETs is 3.9 nm. Figure 1 shows the typical structure of an SP SOI nMOSFET. Figure 2 is the T-SUPREM [11] simulated doping profile along the channel for a 0.1 μm and 0.5 μm device, showing the asymmetric doping along the channel, with heavy doping near the source, and much lighter doping near the drain. A two-step titanium silicidation process with Ge pre-amorphization was used to control the silicide depth and reduce the contact resistance [10].

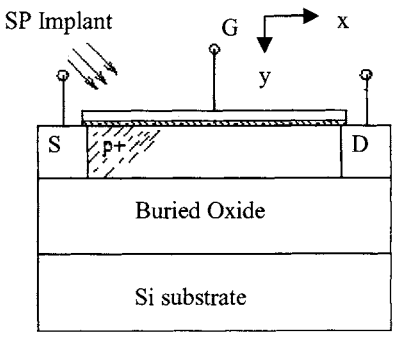

Figure 1. Structure of an SP SOI nMOSFET

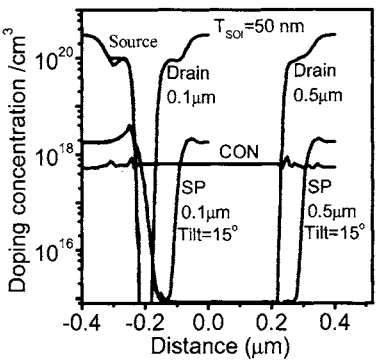

Figure 2. Doping profiles along the channel for SP and CON SOI nMOSFET's 5 nm below the interface along x-direction.

EXPERIMENTAL RESULTS

Both the CON and SP SOI devices were characterized for lateral parasitic bipolar gain β by using GIDL current technique [12]. In the off state when the gate voltage is low or negative and drain field is high, a high vertical field is created in the gate-drain overlap region, causing GIDL currents to flow. The GIDL current is independent of channel length and depends on the area of gate-drain overlap region and the electric field within it. The physical mechanism for GIDL in SOI MOSFETs is identical to the bulk MOSFETs [13]. In the deep depletion region the carriers are generated due to high field, the electrons tunnel towards the drain, whereas the holes move towards the body. However, the holes, unlike in bulk device, cannot flow out from substrate and therefore accumulate in the neutral body. This forward biases the source-body junction, which becomes the emitter-base junction of the parasitic BJT. The hole current is the base current of the lateral bipolar transistor of the MOSFET and gets amplified by the gain of the lateral parasitic BJT. The current gain of the lateral parasitic BJT will increases as the base width (channel length) decreases. As the basic GIDL current is independent of channel length, any enhancement in this current will be proportional to the base width or the channel length of the MOSFET. Channel lengths of more than 4 μm do not provide any current gain [13]. The ratio of drain currents in short channel to long channel device is β+1; hence the value of lateral gain β for parasitic BJT of the short channel MOSFET can be obtained. Further, this technique has the advantage that a body contact is not needed for the characterization of SOI MOSFETs.

GIDL measurements were performed on both SP and CON SOI MOSFETs. The devices were biased with gate at a constant V_G= –2.0V. Drain voltage was ramped and the corresponding drain current was measured for the devices of different channel lengths. The measured drain current is plotted in figure 3 for CON SOI and in figure 4 for SP SOI MOSFETs. Drain current increases with decrease in the channel length, but there is less enhancement of drain current in SP SOI MOSFETs as compared with CON SOI MOSFETs. The long channel MOSFET was taken as 10 μm and the parasitic bipolar gain of 0.20 μm and 0.25 μm devices was calculated for both SP and CON SOI MOSFTs. Figure 5 shows the experimentally evaluated plot of parasitic bipolar gain β versus drain voltage V_{ds} for SP and CON SOI MOSFETs. It can be seen that β is lower in the case of SP SOI MOSFETs for the same channel length. Also it is seen that β increases with decrease in channel length, the reason being that channel length is the base width of the pBJT.

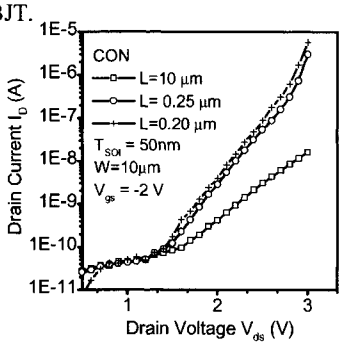

Figure 3. GIDL current enhancement in CON MOSFET for V_G = -2.0 V.

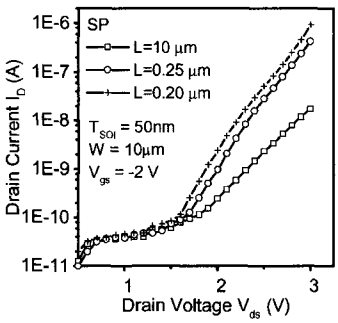

Figure 4. GIDL current enhancement in SP MOSFET for V_G = -2.0 V

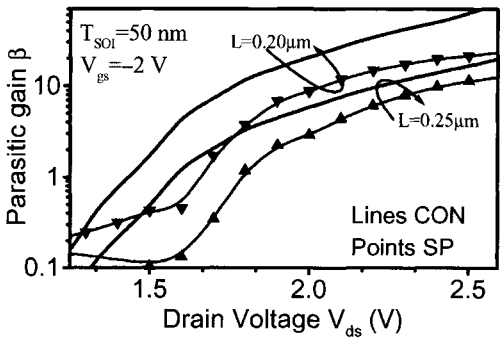

Figure 5. Parasitic BJT gain versus Drain Voltage in CON and SP SOI MOSFETs for 2 different channel lengths

SIMULATION AND DISCUSSION

Simulations were also carried out to understand the lower parasitic gain of SP SOI MOSFET. The simulations were carried out using 2-D process simulator TSUPREM4 and 2-D device simulator Medici [14]. The simulated 3-D plot of impact ionization near the drain junction for L=0.25 μm is shown in figure 6 and figure 7. The bias conditions are V_{ds}=1.2 V and V_{gs}=1 V. It is observed that SP SOI MOSFET has lower rate of impact ionization as compared to CON SOI MOSFETs. This is due to a lower doping in SP SOI near the drain side of the channel. Also it is seen that impact ionization in CON-SOI is concentrated near the surface, whereas in SP-SOI devices much of the impact ionization takes place away from the surface. Since β of the parasitic bipolar transistor is known to be a strong function of the injection currents (due to impact generated carriers), SP-SOI devices are effective in the reduction of the parasitic bipolar action for these MOSFETs.

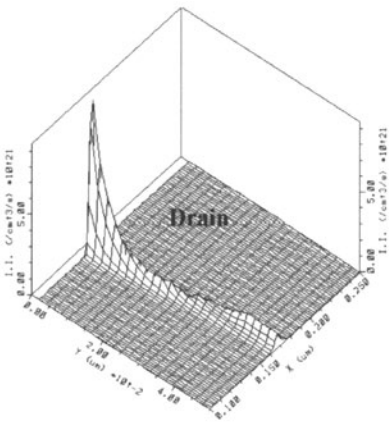

Figure 6. 3–D plot of impact ionization in CON MOSFET

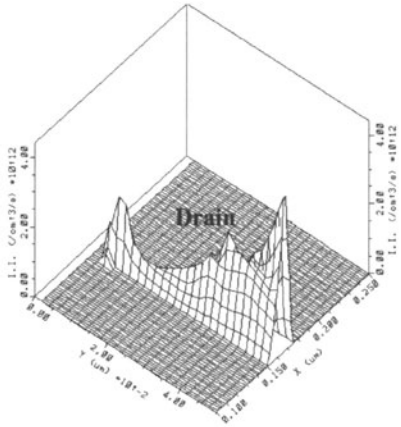

Figure 7. 3–D plot of impact ionization in SP MOSFET

Further insight was obtained by simulating a 'look-alike' BJT based on the SOI n-MOSFET doping for both CON and SP SOI MOSFETs. The structure was generated in the process simulator TSUPREM4 using the actual process parameters and the same process steps as used in simulating the MOSFET. The Poly-gate and the gate oxide were etched away and an ohmic contact was deposited over the body region, which will act as the base contact of the pBJT. This simulated BJT–like structure was used as an input to the device simulator Medici. Default parameters in the device simulator Medici models were used and as such only a qualitative comparison between the two structures can be made. Concentration dependent SRH model was activated in both the structures. The gummel plot was obtained from simulation results for both the CON and SP 'look-alike' BJTs. The gain β as a function of forward bias (V_{EB}) in emitter-base (source-body of the MOSFET) junction is shown in figure 8. As observed the gain in parasitic transistor based on SP technology is lower than that based on CON technology. From the simulated results it was observed that the lower gain in SP based structure is attributed to the pocket doping profile in the body. Peak doping in the body near the source reduces the injection efficiency γ of the parasitic transistor. Also, the heavy doping near the source increases the recombination rate, which reduces the base transport factor α_T. Integrated recombination rate (pairs per sec per micron of depth) was extracted from the simulated output files. In SP SOI the recombination rate near the source junction was one order of magnitude higher as compared to CON. In the body region and near the drain, recombination was slightly higher in CON as compared to SP SOI MOSFET. However the overall recombination rate was almost 7 times higher in SP SOI MOSFET. Hence single pocket doping profile is effective in the reduction of the parasitic bipolar gain for these MOSFETs.

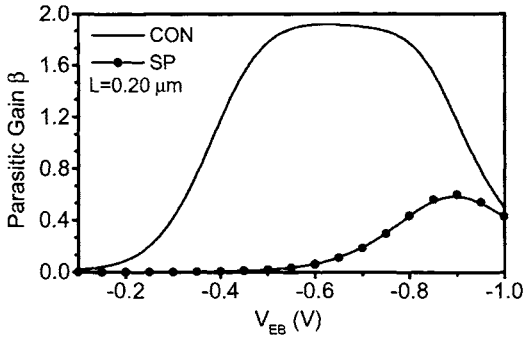

Figure 8. β versus V_{EB} of look alike – parasitic BJT structure of SOI MOSFETs

CONCLUSION

It has been shown that the SP SOI devices has lower parasitic bipolar junction transistor gain which is attributed to the low rate of impact ionization near the drain and the resulting lower injection current levels. Also the peak doping near the source reduces the minority carrier lifetime and injection efficiency. Hence, channel engineering can be an effective means for alleviating the effects due to parasitic bipolar junction transistor in deep sub-micron SOI MOSFETs.

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Microstructural Evolution and Defects in Ultra-thin SIMOX Materials during Annealing

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ABSTRACT

The microstructure of ultra-thin SIMOX depends strongly on implantation dose, energy and annealing conditions. We used TEM combined with AES and RBS to determine the microstructural evolution of SIMOX wafers subjected to various temperatures during annealing. We found that an optimum dose window to produce a continuous buried oxide layer without Si islands is 3.0-3.5×10^{17} O^+/cm^2 for 100 keV. The thickness of the silicon overlayer and BOX layer produced in this dose window was about 170 nm and 75 nm respectively. RBS analysis showed that a high quality crystalline Si layer was produced after annealing at 1350 °C for 4 hrs. The defect density was very low (< 300/cm^2) for all samples implanted at 100 keV.

1. INTRODUCTION

Silicon-on-insulator (SOI) has become a significant technology for high density integrated circuits. For the fully depleted MOSFET devices operating at low-power low-voltage, SOI wafers must have a very thin silicon film and requires a tight thickness uniformity [1-2]. A low-dose low-energy separation by implanted oxygen (SIMOX) is one of the most promising technologies for making an ultra-thin SOI structure. This technology permits a direct formation of an ultra-thin Si active layer with a thin buried oxide (BOX) layer without sacrificial oxidation to achieve the thin film SOI. The low-dose low-energy implantation reduces processing cost and time, thus increasing throughput, and produces fewer defects in the Si active layer. A number of investigations have demonstrated the feasibility to fabricate a very thin SIMOX structure by using low doses [3-5]. However, the correlation between the microstructure and the processing parameters is not well established. In this work, a set of SIMOX wafers fabricated at different doses and energies were characterized using transmission electron microscopy (TEM), Auger electron spectroscopy (AES), and Rutherford backscattering spectrometry (RBS) in order to understand the correlation between implantation dose and energy and the formation of SIMOX structure.

2. EXPERIMENTAL DETAILS

The SIMOX wafers were prepared using the Ibis 1000 high-current oxygen implanter. Oxygen ion doses of 2.5, 3.0, 3.5, 4.5, 6.0 and 8.0×10^{17} O^+/cm^2 were implanted into p-type <100> Si wafers at 100 keV. In order to study the effect of implantation energy on the microstructure of SIMOX, oxygen ion doses of 2.0 and 4.5×10^{17} O^+/cm^2 were also implanted at 65 keV. The wafer temperature during implantation was approximately 560 °C and beam current was about 40 mA. The implanted wafers were transferred to an annealing furnace and were

subjected to ramping up to the temperatures of 1100, 1200, 1300 and 1350 °C with no hold and annealed at 1350 °C for 4 hrs in an Ar atmosphere containing <1% O_2. The ramping rate was 10 °C/min. Microstructures of SIMOX samples before and after annealing were characterized by a Hitachi 8100 TEM operating at 200 keV. The oxygen distribution of as-implanted and the oxygen redistribution during annealing were studied using AES. To investigate the extend of implantation damage and restoration during annealing, Rutherford backscattering and channeling technique with a 2.0 MeV He^+ ion were used in the experiment. A wet chemical etching method and optical microscopy were used to determine the defect density in the Si overlayer of SIMOX samples annealed at 1350 °C for 4 hrs.

3. RESULTS AND DISCUSSION

3.1. Microstructure analysis using TEM imaging

Fig. 1 shows cross-sectional TEM (XTEM) micrographs of SIMOX samples that were implanted at 100 keV and subsequently annealed at high temperature. The as-implanted samples with a dose of 2.5, 3.5, 4.5, 6.0 and 8.0×10^{17} O^+/cm^2 are designated by letters 'A', 'B', 'C', 'D', and 'E', respectively. The surface roughness and the number of voids formed near the surface of the samples increased with increasing dose. Note in Fig. 1 that many multiple faulted defects (MFDs) indicated by arrows are present at the depth of 150-200 nm in all as-implanted samples and no buried oxide layer is formed. With doses above 3.5×10^{17} O^+/cm^2 (Fig. 1 C, D, and E), the striation structure (a mixture of SiO_2 and Si) is observed around the projected range (≈ 224 nm at 100 keV according to TRIM program). After annealing at 1350 °C for 4 hrs in Ar(O_2) atmosphere, the microstructures of annealed samples are shown in Fig. 1 (A-a) (B-a), (C-a), (D-a) and (E-a). It is obvious that an oxygen dose of 2.5×10^{17} O^+/cm^2 is not enough to form a continuous BOX layer. For the dose rage of $3.0\text{-}3.5\times10^{17}$ O^+/cm^2, a well defined continuous BOX layer is formed with no Si islands in the BOX layer. At doses above 3.5×10^{17} O^+/cm^2, a continuous BOX layer is formed with numerous Si islands (Fig. 1 C-a, D-a, and E-a). The density of Si islands increases with increasing dose. It has been suggested that the formation of Si islands is closely related to the striation structure in the as-implanted samples [6]. The thickness of layers measured from these micrographs is shown in Table 1.

The microstructural evolution during ramping and annealing is shown in Fig. 2. TEM images show that in 65 keV sample a continuous BOX layer develops at a lower temperature compared to 100 keV. This is due to the reduced straggling of implanted oxygen. Upon annealing the number of oxide precipitates decreases with increasing temperature, and the oxide precipitates grow through the "Ostwald ripening" process. This facilitates the redistribution of the implanted oxygen toward the buried oxide layer [7-8]. Note that an oxide layer is formed in 65 keV samples during the ramping process. Silicon interstitials generated by both cascade collision and internal oxidation will migrate toward surface and into the substrate. If a BOX layer is present, Si interstitials can not easily migrate through the BOX layer due to the very low diffusivity of Si in SiO_2, thus the surface is the only sink. This may explain the higher dislocation density in these samples compared to 100 keV samples. Note in Fig. 2 (D) that a defect is pinned between oxide precipitates and not visible at 1300 °C. The pinning of dislocations into the oxide precipitates may prevent the growth of defects and lead to