PART I

Deposition

POLY-Si - A MOST IMPORTANT MATERIAL

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ABSTRACT

The many advantages of polycrystalline Si (poly-Si) to semiconductor device manufacturing are reviewed, together with methods of deposition and new uses.

INTRODUCTION

Because of the major role played by poly-Si in MOS device technology, the title of this paper was originally based on a contraction of Metal-Oxide-Semiconductor-Transitor (MOS-T). This limited view does not reflect the widespread and essential use of poly-Si in virtually all types of semiconductor devices. [1]

ADVANTAGES OF POLY-Si

Understanding and utilizing the advantages offered by poly-Si was one of the most important fundamental developments in the history of integrated circuits. Poly-Si is so useful because it:

- Forms an adherent oxide
- Absorbs and re-emits dopants
- Has good step coverage if deposited by CVD
- Matches mechanical properties of Si single crystal
- Has a high melting point
- Has a compatible work function for MOS devices
- Absorbs heavy metals (gettering)
- Forms high conductivity silicides
- Is compatible with HF

These properties make poly-Si uniquely suited to be a primary local interconnect material, and its ability to form silicides extends that application to longer interconnect lines. Its compatibility with IC processing and its good step coverage provided by CVD offers many advantages in bipolar, MOS, and biCMOS circuits, because it:

- Provides low MOS threshold voltage
- Fills trenches
- Permits SAliciding
- Provides long gate oxide wear-out times
- Provides a wide range of resistivities
- Permits oxide reflow process temperatures
- Simplifies processing
- Can be selectively deposited
- Permits shallow, high quality junctions
- Forms silicide thin film resistors

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These advantages have resulted in many device applications, including:

- Self-Aligned MOS Gates
- Source/drain contacts
- Multilayer interconnects
- Dielectric isolation
- 3-D structures
- Non-volatile floating gates
- Fusible links
- Emitter & base contacts
- Thin film devices
- Emitter diffusion source

DEPOSITION OF POLY-Si

A wide range of deposition techniques for poly-Si have been investigated.[1] In the early stages of development (1963-1970), physical vapor deposition (PVD) techniques were used; however, x-ray and ion damage, unwanted impurities, non-uniform step coverage, ±5-10% thickness variations, and low productivity per capital cost prevented widespread use of these methods.[2]

In the early manufacturing period (1970-1976), cold wall, atmospheric pressure "epitaxy" reactors were used for poly-Si deposition. Such reactors offered thickness variations of ± 5-10% and low productivity per capital cost. The H_2/SiH_4 process at 910°C provided a large grain size after deposition. The N_2/SiH_4 process at 650°C offered smaller grain size, but much worse uniformity. Even with these limitations, Si gate PMOS and NMOS ICs became a major factor in the semiconductor device market in the early 1970s.

The LPCVD process [3], first introduced commercially in 1976[4-7], revolutionized poly-Si deposition and set the stage for MOS ICs to become the dominant device type. This diffusion furnace process (SiH_4, 625°C, 0.4 torr, 3/16-inch wafer spacing) reduced deposition costs more than 90%, improved uniformities to ±1-2%, and provided the optimum grain structure for good post-deposition doping control. As a result, yield of MOS ICs was markedly improved, while production costs were reduced.

This LPCVD process, with minor variations in reactor geometry, has been the primary means of poly-Si deposition for ICs during the last 14 years, and it shows every indication of continuing this dominance for many years to come.

ALTERNATIVES TO LPCVD

Alternatives to the LPCVD process being considered today include:

- Rapid Thermal Processing CVD (RTPCVD) and Annealing[8]
- Cold wall, reduced pressure (10-200 torr) CVD[9,10]
- Hot wall, higher temperature (850°C) CVD[11]

RTPCVD techniques include Limited Reaction Processing (LRP) in which the reactant gases are present in the reactor and rapid heating/cooling of the wafer is used to start/stop the reaction.[12] Conventional CVD with rapid heating has also been studied.

In a related technology, rapid heating/cooling has been used to decrease sheet resistance by freezing in non-equilibrium concentrations of dopant.[13]

RTPCVD techniques are usually limited to single wafer reaction chambers, and productivity per capital cost can become an issue. Lower temperatures (600-650°C) provide the desirable grain size but unacceptably low wafer throughput because of the inherently low growth rate. Conversely, higher temperatures (900-1000°C) provide higher productivity, but with an undesirable, large, grain size. Multiple steps (low temperature nucleation with higher temperature growth) offer some compromises.[8]

Growth of poly-Si on oxide creates time-varying surface emissivity, and this can drastically effect wafer temperature in RTPCVD. This, and variable backside emissivity, can adversely effect RTPCVD results.[8]

RTPCVD does offer a convenient means for load-locked processing, which can provide in-situ cleaning and depositing multiple layers.[8]

Cold wall, reduced pressure CVD is usually reserved for blanket epitaxial silicon deposition. This style reactor can also be used to deposit:

- Epitaxy layers selectively deposited in windows cut through field oxide[14]
- Poly-Si layers selectively deposited in windows cut through field oxide[15]
- Selective epitaxy with uniform poly-Si deposited on top of the field oxide[16]
- Blanket epitaxy with regions of poly-Si nucleated on islands of oxide or nitride[17]
- Blanket epitaxy with high quality single crytal silicon growing laterally out from windows cut through field oxide[18]

Conventional silicon epitaxy typically requires temperatures above 950°C to assure good crystal quality. The temperature for low defect density epitaxy has been pushed down to 750°C and even lower. No significant commercial use of this capability has been made because growth rates at temperatures below 850°C are very low (<0.05 um/min) and defect densities can be very high.[19]

Device applications using poly-Si or selective poly-Si usually require rather thin layers (<10,000A); therefore, cold wall CVD of poly-Si in the 800-900°C range has been commercially significant.[20]

Hot wall, higher temperature (850°C) LPCVD at higher pressures (0.5-5 torr) and larger wafer spacing (>3/16-inch) offers the interesting possibility of higher growth rates for blanket epitaxial growth, selective epitaxy, and selective poly-Si deposition.[11] This deposition technique is still in development and has not been put into commercial use.

For all its challengers, conventional 600°C LPCVD in a horizontal or vertical diffusion furnace continues to be the dominant deposition technique for poly-Si because the challengers have yet to offer a clear-cut yield benefit. As a further advantage, LPCVD reactors operate in the surface reaction limited regime at low pressure which permits filling of the deep trenches or stacked capacitor cavities that are required for advanced CMOS memory devices.

Some of the challengers offer new capabilities that are not available by conventional LPCVD, and such capabilities may have significant commercial advantage. Such capabilities include:

- Selective deposition
- Multilayer, sequential, in-situ deposition with special cleaning and etching steps

NEW DEVICE APPLICATIONS FOR Poly-Si

New device applications for poly-Si include:

- Poly-Si contacts that:
  - eliminate Al alloy spiking[21]
  - provide high quality, extremely shallow junctions[22]
  - permit high gain emitters in bipolar devices[23]
- Selective deposition for:
  - Local interconnect straps[20]
  - Via and contact plugs[24]
  - 3-dimensional structures[25,26]
- Simultaneous deposition of blanket epitaxy with poly-Si nucleating on oxide islands to create high diffusivity regions[17]
- Trench fill[20]
- Stacked capacitors[27]
- Self-Aligning Silicide[28]

- Thin Film Devices[29], such as:
  - Thin film diodes and transistors for displays
  - Thin film transistors for active connectors in 3-dimensional ICs
  - Solar cells[30]
- Microcircuit transducers[31-33], such as:
  - Pressure sensors[31,32]
  - Strain Gauges[32]
  - Vapor sensors[32]
  - Mechanical components[33]

THE FUTURE

Poly-Si will have applications in semiconductor devices far into the future because it is plays a major role in the fabrication of all manner of devices:

- MOS	- CMOS
- BiCMOS	- Bipolar
- Transducers	- Displays
- Dielectric isolation	- Solar Cells
- 3-dimensional ICs	- Thin Film Devices

The challenges for LPCVD are:

- Native oxide removal (where required)
- Grain structure and doping control
- Enhanced conductivity
- Integrated, multilayer processing
- Larger diameter (250 and 300mm) wafers

Poly-Si will, indeed, be a most important material for semiconductor devices well into the 21st century.

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INTERFACE OXIDE FREE POLY SILICON DEPOSITION USING IN-SITU HF CLEANING PROCESS

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ABSTRACT

A LPCVD polysilicon deposition with in-situ anhydrous HF cleaning process has been developed. The deposited polysilicon and interface properties have been characterized using SIMS, XTEM, RBS, and Auger analysis. The results indicate that an interface oxide free polysilicon deposition using conventional LPCVD furnace can be achieved by careful design of in-situ anhydrous HF cleaning process. After short time rapid thermal annealing, random and channel RBS studies show that most of the deposited polysilicon is epitaxially aligned with silicon substrate and there is no oxide ball up phenomenon. Twinning structure was observed under TEM. No impurity segregation at the poly-mono silicon interface confirms that the interface is oxide free. Possible applications of this polysilicon process include polysilicon emitter contact for high speed bipolar technology and source/drain contacts for MOS devices.

INTRODUCTION

For almost two decades, polysilicon has been used in metal oxide semiconductor (MOS) and bipolar silicon technologies[1]. In recent years, polysilicon emitter bipolar devices have driven high performance (high speed and high driving ability) VLSI technologies. In a recent report, an pnp transistor with cut off speed up to 27 GHz has been obtained[2]. Critical process steps of this high speed pnp include polysilicon emitter and optimized emitter, base, and collector dopant profiles. The successful use of polysilicon in high performance devices depends on proper control of polysilicon structure and the poly-mono silicon interface properties. An intentional poly-mono interface oxide ~20Å has been proven to increase transistor gain[3]. In other aspect, interface ball up is required to assure low emitter resistance for high speed bipolar devices. The interface ball up is a strong function of post deposition heat treatments and the nature of the interface oxide. It is difficult to have tight control in a production environment for this interface ball up.

This paper describes a novel low pressure chemical vapor deposition (LPCVD) of polysilicon with in-situ anhydrous HF cleaning process. The purpose of this process development is to obtain an interface oxide free polysilicon deposition for high speed bipolar applications. The properties of poly-mono silicon interface are characterized using secondary ion mass spectroscopy (SIMS), cross section transmission electron microscopy (XTEM), Rutherford backscattering spectroscopy (RBS), and Auger analysis.

EXPERIMENT

A three zone traditional LPCVD furnace is used in this study. The anhydrous HF is connected as one of the process gas. The Si source is SiH_4. After RCA cleaning, the samples are dipped with 100:1=H_2O:HF. The process pressure is 300 mTorr and the process temperature is set at 625°C. The polysilicon deposition rate is 50-60 Å/min. Anhydrous HF gas is used in this system as initial etch of native oxide. Silane and HF are introduced following HF

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initial etch step to make sure that surface of the sample is oxide free before main deposition process.

In this study, a batch of boron doped, p-type CZ substrate with resistivity 4-15 Ω-cm is used as the starting material. The thickness of deposited polysilicon varies from 200 to 400Å After polysilicon deposition, selective wafers are implanted with BF_2. The implantation energy is 15 KeV and the dose is 4×10^{15} /cm^2. Some wafers are subjected to AG-210 rapid thermal process at temperature varies from 1030 to 1130°C and time ranges from 8 to 30 seconds. The annealing ambient is dry nitrogen. SIMS measurement is used to monitor the boron (B), fluorine (F), and oxygen (O) signals through the poly-mono silicon layer. It was proven[4] that the interface oxide has strong tendency for the segregation of dopant as well as oxygen and fluorine. Auger analysis, RBS, and XTEM are used to verify these results.

RESULTS AND DISCUSSION

SIMS Measurement

All SIMS data were taken on a Cameca IMS-3F with an O^{2+} primary beam. Figure 1 shows boron (B), fluorine (F), and oxygen (O) signals of wafer with 50 cc/min in-situ HF polysilicon deposition and BF_2 implantation. The heat treatments after polysilicon deposition and BF_2 implantation are 1130°C for 8 second and 1090°C for 21 second. In these SIMS profiles, only a set of signal peaks close to the surface is observed. This set of signal peaks corresponds to the effective boron range. Note that no evidence of any interface oxygen rich region can be observed from these SIMS profiles. With HF flow rate of 150 cc/min, similar SIMS profiles are obtained.

SIMS measurement on samples which have polysilicon deposited without in-situ HF cleaning is shown in Fig. 2 for comparison. In Fig.2, the rapid thermal process is 1070°C for 30 second. There are two sets of B, F, O signal peaks. Close to the surface, the signal peaks are mainly due to the surface oxide as shown later on RBS and Auger analysis. However, the signal peaks of B, F, and O at depth of 340Å strongly suggest that an oxygen rich poly-mono interface layer exists.

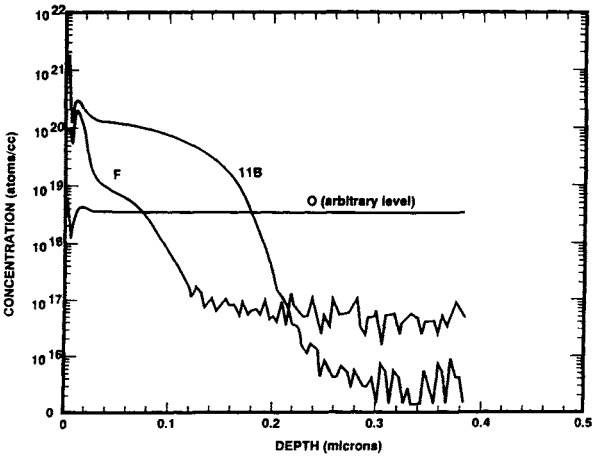

Figure 1. SIMS profile of B, F, and O on sample with 50 cc/min in-situ HF polysilicon deposition, BF_2 implantation and RTA annealing.