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Transistor Scaling—Methods, Materials and Modeling

Editors: Scott Thompson, Faran Nouri, Wen-Chin Lee and Wilman Tsai

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PREFACE

For the past four decades, geometric scaling of silicon CMOS transistors has enabled not only an exponential increase in circuit integration density — Moore's Law — but also a corresponding enhancement in the transistor performance. Simple MOSFET geometric scaling has driven the industry to date. However, as the transistor gate lengths drop below 35 nm and the gate oxide thickness is reduced to 1 nm, physical limitations such as off-state leakage current and power density make geometric scaling an increasingly challenging task.

In order to continue CMOS device scaling, innovations in device structures and materials are required and the industry needs a new scaling vector. Starting at the 90 and 65 nm technology generation, *strained silicon* has emerged as one such innovation. Other device structures such as multi-gate FETs may be introduced to meet the scaling challenge.

Symposium D, "Transistor Scaling—Methods, Materials and Modeling," held on April 18-19 at the 2006 MRS Spring Meeting in San Francisco, California, had 54 oral and poster presentations, including eight invited papers from industry and academic leaders. The symposium brought together materials scientists, silicon technologists and TCAD researchers to share experimental results and physical models related to state-of-the-art MOSFETs, and to discuss the new and innovative approaches necessary to continue the transistor scaling. This volume contains expanded versions of many of these presentations in the areas of technology development, metrology, characterization and modeling.

We wish to thank all our invited speakers, our contributors and our participants for a lively and stimulating symposium. We also gratefully acknowledge the financial support from TSMC, Ltd.

Scott Thompson
Faran Nouri
Wen-Chin Lee
Wilman Tsai

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