Joint Session: System in Package

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Silicon Based System-in-Package : Breakthroughs in Miniaturization and 'Nano'-Integration Supported by Very High Quality Passives and System Level Design Tools

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ABSTRACT

The very large development of home and domestic electronic appliances as well as portable devices has led the microelectronics industry to evolve in two complementary directions: "*More Moore*" with the continuous race towards extremely small dimensions, hence the development of SoCs (System on Chip) and more recently a new direction that we could name "*More than Moore*" with the integration of devices that were laying outside the chips and here the creation of SiPs (System in Package).

These two approaches are not in competition with one another: this paper will show some examples of integrated nano-systems that use several SoCs.

The technology we have developed is called Silicon-Based System in Package.The first products using this technology are now in volume production and used mainly in the field of wireless communication.

This new technology relies on four pillars. Passive integration is the first: very efficient and high quality factor capacitors and inductors have been integrated, allowing the creation of complete modules including active devices, filters and decoupling capacitors. High-density MOS capacitors with 1-1000 nF capacitance, and as high values as 25-250+ nF/mm^2 specific capacitance have been fabricated in 150 mm diameter Si-wafers, containing over 1 billion macropores. Typically an ESR less than 100 mΩ and an ESL less than 25 pH were found for capacitors over 10 nF. This novel concept is an important step forward in improving the stability of power-amplifier modules by replacing conventional SMD technology.

Whereas generations with capacitor densities of up to 100 nF/mm² will be using "conventional" materials and structures, the next steps in the roadmap will call for new 3D structures and materials such as high-k dielectrics.

The second element is advanced packaging. New technologies, such as the assembly of silicon chips onto other silicon chips, also named "double flip-chip" have been developed. This has been made possible thanks to the combination of the most advanced microbumping and die placement techniques. In addition to a tremendous reduction of size (up to a factor of 10 to 20) these techniques have also brought a better repeatability of system performance.

The third element has been the development of design tools that allow a seamless system design for engineers used to IC design tools and flows. Our Design Environment allows co-design of multiple-technologies chips and their integration in a single system. This IC-like Design Environment has greatly contributed to the adoption of the technology.

Testing is the fourth element and is one of the economical enablers of the technology. The key words are: "Known-Good-Die", RF test, system test, etc. Some innovative RF probing and full on-wafer subsystem testing will be shown. Even though efficient testing is not vital for the technical feasibility of this system integration, it becomes very quickly one of the most important enablers, especially when we deal with very high volumes of production. The conclusion of the paper will be an open door to the future. Some innovations like the integration of solid state lighting devices or even energy storage devices inside our SiPs will be presented.

INTRODUCTION

Looking for the lowest cost per digital function has led the semiconductors industry to innovate in the field of miniaturization at the individual device level, like decreasing the length of individual transistors to less than 20 nm and the surface area of memory cells to less than 1 μm^2. Since these technologies are using more and more complex process steps, materials and lithography techniques, the initial investment costs to create a new product have increased tremendously. This leads to more and more generic and programmable chips. These products are usually called Systems on Chip (SoC). Whereas this approach seems to be economically efficient when dealing with data processors, this standardization or even commoditization does not allow any product differentiation except through their embedded software or through their operating software. In addition, this miniaturization requires the use of more and more passive components such as inductors and capacitors that currently take up most of the printed circuit board area in consumer products for instance [1]. As these passive devices do not scale by Moore's law, their integration into SoCs turn into a non cost-effective solution. Separate integration of those passive devices is an interesting alternative: it allows to optimize both the passive and active devices on different technology platforms and to exploit this separate platform to integrate technologies that cannot be properly combined with advanced CMOS. For example, integration of MEMS or sensors becomes easier and cheaper [2]. One of the answers brought to this paradigm is heterogeneous integration of multiple dies in a single package, also called System in Package (SiP). This multiple die integration is not new in itself but we have helped create a breakthrough thanks to efficient die-to-die interconnection processes as well as system level design that allows to integrate complex functions into standard miniature packages. This breakthrough was made possible thanks to the parallel development of the four following technology elements: passive integration, advanced packaging, advanced testing and system level multiple technology design. This is shown in Figure 1. The deployment of this program is what has been named "*More than Moore*".

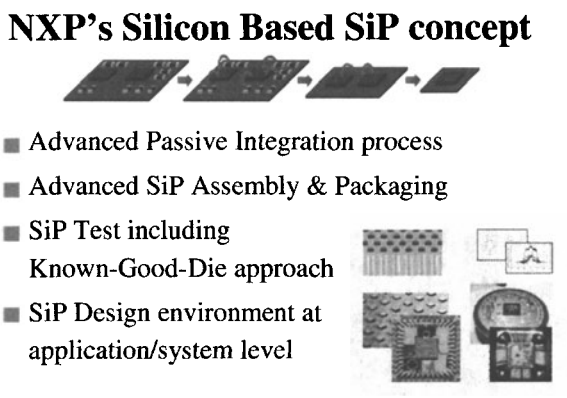


Figure 1. The four elements of NXP's SiP approach.

Many articles try to determine which solution is going to be the best between the SiP and SoC approaches. We prefer to present these two approaches as complementary ones. It is now clear that the SoC approach is the best suited one when we want to lower the cost per digital function. This is true for high volume products like microprocessors, standardized products like video or sound codecs, etc. When we want to integrate more flexible responses to more specialized products and when we look at the highest value per total system then the SiP approach seems to be the most efficient: it allows to integrate several either already existing and/or dedicated dies together to create a new function without having to pay for long product development times and very expensive masksets. Figure 2 shows an example of a recent Bluetooth radio module containing both kinds of products.

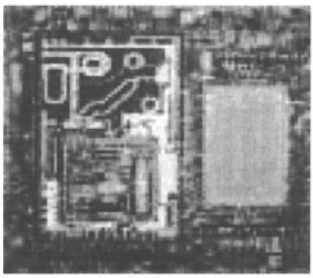


Figure 2. Integrated Bluetooth communication module including several SoCs (radio on the left, baseband processor on the right).

Figure 3 shows another example where three existing SoCs using advanced CMOS have been combined in a single package to create a breakthrough in the size of a Set Top Box by creating a One Chip Set Top Box. In summary, we think that, at least during another five to ten years, the two approaches will be complementary.

As indicated in the introduction, this approach is based upon four balanced pillars that were developed in parallel.

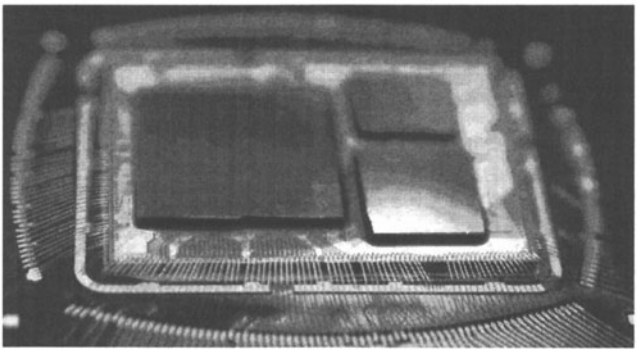


Figure 3. Single-package Set Top Box including three active dies from different technologies (CMOS090 left, CMOS18 on the bottom and QUBiC4+ BiCMOS top right) assembled onto a passive die.

PASSIVE INTEGRATION

Passive integration is the first piece of the puzzle. It is very interesting in terms of miniaturization, but also in terms of performance. Very efficient and high- quality factor capacitors and inductors have been integrated, allowing the creation of complete modules including active devices, filters, decoupling capacitors. Some examples will be shown, in particular in the field of connectivity and cellular phones.

The solution proposed is the use of a substrate or interconnection die carrying the passive devices. The technology used for the making of this die is called PICS (for Passive Integration Connecting Substrate).

A. Capacitors

High-density MOS capacitors with 1-1000 nF capacitance, and as high values as 25-250 nF/mm2 specific capacitance have been integrated in macroporous Si-wafers, containing over 1 billion macropores [3-5].

To reach these high values, we have made the choice to use the third dimension inside the silicon. The structure of the integrated capacitors is shown in Figure 4.

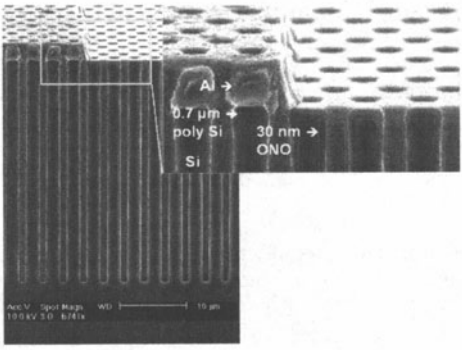


Figure 4. Structure of 3D macro-pores in PICS capacitors.

The use of the third dimension allows us to reach these values with dielectric layers manufactured using conventional front-end techniques like CVD and thermal processing, hence the very high quality of these layers. This was preferred to high-k materials grown with lower temperature processes since these often lead to higher defect densities. Today, these high-k materials also show some significantly lower quality factors than conventional oxide/nitride in MOS structures because of dielectric losses and piezoelectric relaxation phenomena inside the material.

Superior decoupling performances in the GHz range have been shown. Typically a series resistance of less than 100 mΩ and a parasitic inductance of less than 25 pH were found for capacitors over 10 nF [3]. This novel concept can be an important step forward in improving the stability of power-amplifier modules by replacing conventional SMD technology.

Figure 5 shows the various nodes in the passive integration roadmap that we have set up.

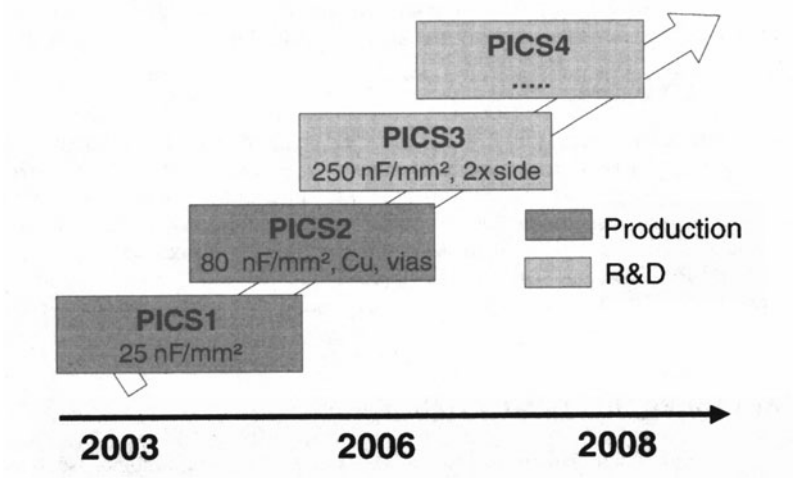


Figure 5. Silicon-based Passive Integration Roadmap.

The generations with capacitors density of up to 100 nF/mm² will be based on using "conventional" materials and processes.

Values of up to 250 nF/mm² have been reached with these materials, thanks to the optimization of the developed surface. The next steps in the roadmap will call for new materials such as higher-k dielectric layers and new process steps, in combination with 3D structures.

B. Inductors and Resistors

Resistors are simply made by using the poly-Si top electrode of the capacitors. This well-controlled doped layer is well suited for the resistors values needed in the subfunctions that we need to integrate.

Inductors are made by using the two metal layers also used for interconnects. Single-turn coils are mainly made from the thick (up to 10 µm) second metal and multi-turn coils are made from the two layers for cross-over. This second metal layer is using standard aluminum-based alloys as well as copper. The choice between Al and Cu is dictated by the need for very high quality factors and low resistance values. Q factors of up to 40 (@ 1 GHz) have been demonstrated for several nH inductor values.

The combination of these three types of passives enable the realization of multiple passive functions such as filters, decoupling capacitors, RC and low pass filters, etc. All these functions, combined with one or several active dies have demonstrated their importance, not only in RF applications but also in many other applications where miniaturization counts. Figures 3 and 7 show some examples of products that are manufactured today in large quantities. Several examples have also been recently announced or published.

C. Modeling

Bearing in mind that from the very beginning of this SiP R&D activity we had planned to develop these passive technologies together with IC-like design tools, we have made the choice to develop models that were compatible with this kind of design flow. Whereas models for capacitors and resistors are quite simple, we have used also compact and predictive models associated with scalable inductor layouts to simplify the design and make the simulations more accurate [6]. The combination of this approach with the use of IC-like design tools has led to the creation of passive devices libraries with many kinds of scalable devices (p-cells).

ADVANCED MICRO-PACKAGING

The second element is advanced packaging. New technologies, such as the assembly of silicon chips onto other silicon chips, also referred to as "*double flip chip*" have been used [7-9].

This has been made possible thanks to the combination of the most advanced microbumping and die placement techniques. Examples are shown in Figure 3 and Figures 6-7 where cross-sections of products and top views are presented.

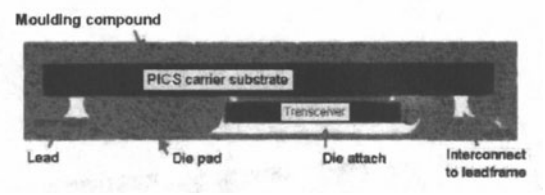
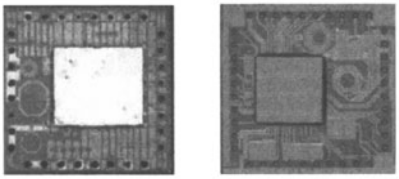


Figure 6. Cross-section of a fully integrated radio module in a moulded leadframe. (Compare Fig. 7).



(a) (b)

Figure 7. Examples of SiPs: (a) Bluetooth communication module and (b) GSM transceiver.

In addition to a tremendous reduction of size (up to a factor of 10 in area and more than 50 in volume) these techniques have also brought a better repeatability of system performance, thanks to a well-controlled placement of passive functions and to the possibility to tune the passive components to the really needed value.

DESIGN AND SIMULATION TOOLS AND SYSTEM TEST

Design Environment

The third element has been the development of design tools that allow a seamless system design for engineers used to IC design tools and flows.

Our Design Environment allows codesign of multiple-technologies chips and their integration in a single system. The first level is at individual passive devices level: like in the usual IC technologies, compact models, elementary libraries and libraries of more complex functions have been developed. The second level is at physical level: packaging and interconnections between the dies are part of the design flow. The third level deals with the electromagnetic, thermal and mechanical behaviors of the different dies inside the package. An example of thermal-mechanical simulation is shown in Figure 8.

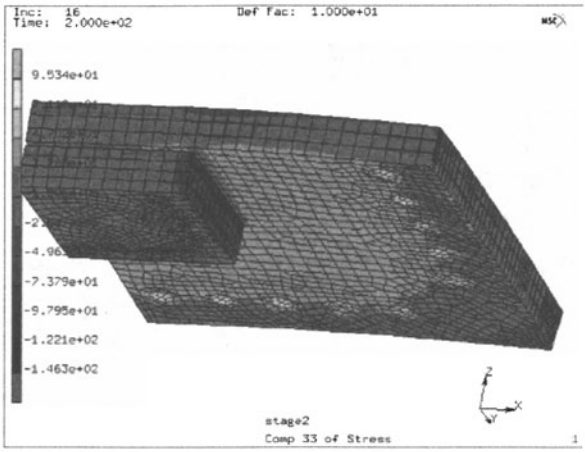


Figure 8. Example of a thermo-mechanical simulation (representation of z-axis shear stress) to identify the critical areas in the product design.

The complete approach is called Multi Technology Design Environment. It uses dynamic links between the various product databases and allows software based verification and error checks.

Finally, this IC-like Design Environment has contributed considerably to the adoption of the technology.

Testing of SiPs

Testing is the fourth element and is one of the economic enablers of the technology.

Some innovative RF probing and full on-wafer subsystem tests have been developed. For example, passive dies used with the active devices are brought as closely as possible to the die probes, hence reproducing the operating environment of the active dies. It gives back values that are very close to those of the die "alone". These technologies allow us to obtain "Known Good Dies" at wafer level.

Even though efficient testing is not vital for the technical feasibility of system integration, it becomes very quickly one of the most important enablers, especially when we deal with very high volumes of production.