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GaN Based Electronic Device and Sensors on Silicon

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GaN-on-Si HEMTs: From Device Technology to Product Insertion

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ABSTRACT

In the last decade, GaN-on-Si has progressed from fundamental crystal growth studies to use as a platform technology for a line of reliable, commercially availability RF power transistors. This paper will briefly review progression of the GaN-on-Si material system and device processing, then present performance of the technology for commercial and military RF wireless applications.

INTRODUCTION

Future modulation schemes and air interfaces for mobile wireless communications require base stations with several watts of linear output power and instantaneous bandwidth up to 15% at frequency bands extending to ~6 GHz. Translated to the transistor level, this implies excellent linearity and thermal stability with simultaneous high power and high frequency capability. Additionally, advanced switch-mode amplifier architectures require output stage power transistors with cutoff frequencies >20 GHz and high voltage capability to support drain modulation designs. Military communications (e.g., JTRS - Joint Tactical Radio System) and electronic warfare (e.g., broadband jammers) systems also present significant challenges due to requirements of high output power and bandwidth up to or exceeding one decade. In such units, highly efficient broadband power transistors can reduce component count and decrease weight and/or footprint.

Appropriately designed GaN-on-Si HEMTs are excellent candidates to meet the performance targets in commercial and military insertion opportunities described above. The GaN material system has long been lauded for its high frequency and power handing capability. The HEMT structure provides excellent transconductance and linearity. GaN-on-Si offers GaN performance attributes in a cost-competitive platform. While the high-quality, low-cost, and large-diameter of Si substrates are well understood, other inherent advantages of GaN-on-Si include the ability to leverage established Si processes for wafer grinding & polishing, via-hole formation, and AuSi eutectic die attach.

Through thermal design and advanced packaging, thermal management of GaN-on-Si – sometimes cited as a limiting feature of the technology – can reach levels similar to GaN-on-SiC. High frequency operation has been demonstrated in both discrete and MMIC implementations. A family of packaged GaN-on-Si power transistors has been qualified and commercially released. These products operate at frequencies from DC to 6GHz and voltages up to 28V. Qualification of a product family operating to 48V is in

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progress and will extend the power levels and bandwidth of the existing 28V products, enabling high power, extremely portable systems. Such devices will facilitate improved communications transmit distance and extend the umbrella size of electronic protection units.

MATERIAL GROWTH AND DEVICE PROCESSING

All Nitronex GaN-on-Si products are grown by MOCVD on 100 mm float-zone Si (111) substrates. Proprietary, strain-compensating (Al,Ga)N transition layers and an amorphous $Si_xAl_{1-x}N_y$ nucleation layer are employed to accommodate lattice and thermal expansion mismatch between the substrate and the epilayers. Proper AlN nucleation conditions and reactor flow dynamics during GaN growth have been shown to play a critical role in overall device performance. Optimization of these has significantly reduced microwave loss to the substrate [1] and has improved RF power and efficiency of HEMTs [2]. Growth conditions have been optimized to result in a high level of thickness uniformity across the 100 mm substrate. Typical thickness uniformity of the stack is ~5% with 5 mm edge exclusion. 2DEG sheet resistance uniformity is <5%. Surface roughness as measured by 5 µm x 5 µm AFM scan is typically in the 5 - 10 Å. Threading dislocation density as measured by both XSTEM and AFM is $\sim 2 \times 10^9$ cm^{-2}.

Various $Al_xGa_{1-x}N$ barrier layers have been explored, ranging in composition from $x = 0.2$ to 0.3 with barrier thicknesses from 160 - 300 Å. The epi structure used for all products consists of a 180 Å $Al_{0.26}Ga_{0.74}N$ barrier and thin GaN capping layer. All layers of the material stack are nominally undoped. Transport characteristics of the channel have been evaluated by several methods. Room temperature Hall measurements result in 2-dimensional electron gas (2DEG) mobility of 1500 cm^2/V-s range and sheet charge density of 8.5×10^{12} cm^{-2}. Typical 2DEG sheet resistance of a passivated van der Pauw cross-bridge structure is 490 Ω/square.

HEMT fabrication begins with Ti/Al/Ni/Au (250Å / 1000Å / 400Å / 1500Å) ohmic metallization and RTA in flowing N_2 at ~850ºC. Devices are immediately passivated in by SiN_x PECVD deposition at 300°C baseplate temperature. The passivation step is followed by a nitrogen ion implantation step to define active areas of the device. The implant was simulated to produce $>10^{20}$ cm^{-3} vacancy concentration from the surface to a depth of ~0.5 µm. Energy / dose conditions are 30 keV / 6×10^{12} cm^{-2}, 160 keV / 1.8×10^{13} cm^{-2}, and (doubly-charged) 400 keV / 2.5×10^{13} cm^{-2}. Typical sheet resistance of implanted material is $\sim 10^{11}$ Ω/square. Ion implantation has previously been shown to produce highly isolated material regions with resistivity unaffected by subsequent device processing steps. Additionally, implantation produces a planar surface more conducive to MMIC realization.

Openings for gate metallization are formed by a low-damage ICP plasma etch of the SiN_x passivant. The etch accurately transfers a 0.5 µm gate CD to the underlying (Al,Ga)N surface. Etch conditions include 3 W RF power and 60 W ICP power with 20 sccm flowrate of SF_6. This process typically achieves ~3% etchrate uniformity. Schottky gates of Ni/Au (200Å / 5kÅ) are deposited by a separate lithography step to allow overlap of the gate metallization onto the surface of the passivant, forming a dielectrically-defined T-gate that can be optimized to reduce peak electric field. A PECVD SiN_x encapsulation layer is then deposited to protect the device and serve as the

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capacitor dielectric for source field plate (SFP) deposition. The source field plate is deposited by evaporation and extends from the source contact – over the gate electrode – and terminates in the midpoint of the drift region. The SFP was optimized to reduce RF dispersion as measured by pulsed-DC and load pull measurements. The SFP reduces feedback capacitance, and thus increases microwave gain, relative to devices with field plates formed by overlap of the gate electrode on the SiN_x passivant. Devices are interconnected by electroplated Au airbridges to complete frontside processing. A cross-sectional micrograph of the active regions of a GaN-on-Si HEMT is shown in Figure 1.

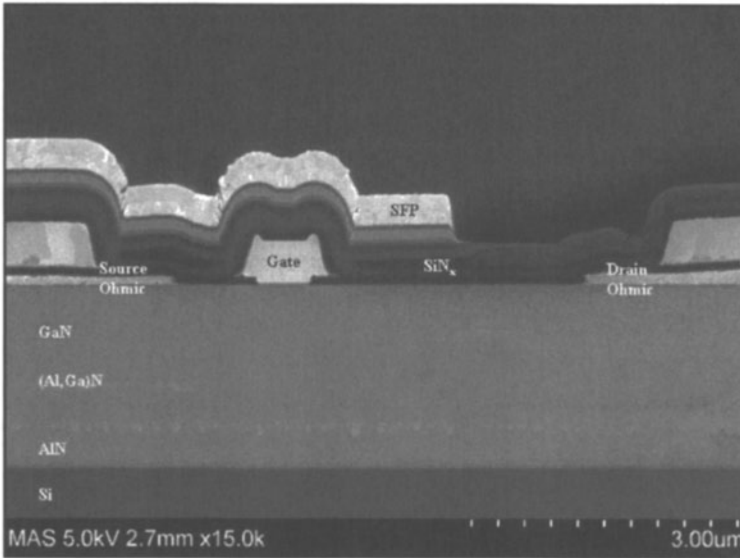

Figure 1. Cross-sectional STEM of GaN-on-Si HEMT, showing epilayers and device construction.

Backside processing consists of grinding and CMP using standard Si techniques. Final wafer thickness is product-specific, and products with chip thickness as low as 2 mils are under development. Through-wafer vias are formed Bosch etch and exhibit near-vertical sidewalls. Frontside source pads are grounded to the backside of the wafer by sputtered seed metal deposition and thick Au backside electroplating. All wafer are probed and screened for both DC and RF performance.

Packaging solutions include low-cost plastic SOIC and thermally-enhanced LDMOS-style air cavity outlines, providing a broad cross-section of performance and pricing options.

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GaN-on-Si IN LOW-COST PLASTIC PACKAGING

The economics of GaN-on-Si combined with low-cost plastic packages enable GaN performance to reach price points required for many driver and pre-driver stage applications, areas not often considered for GaN devices. The plastic packaging process utilizes a copper heatsink, thermally-conductive and electrically-conductive epoxy die attach, and RoHS-compliant plastic overmolding. Figure 2 gives an overview of the plastic package and assembly.

SOIC-based products are available with peak power levels ranging from 5W to nearly 50W. NPTB00004 is a general purpose broadband transistor rated for operation from DC - 6GHz. Large-signal RF performance from 900MHz to 3500MHz measured in load pull is shown in Figure 3. Optimizing source and load impedance for each frequency shown in Fig. 3 produces 5 - 7 W output power across this range. When operated under 2500 MHz WiMAX modulation (single carrier OFDM waveform 64-QAM 3/4, 8 burst, continuous frame data, 10MHz channel bandwidth, peak/avg. = 10.3dB @ 0.01% probability on CCDF) at 2% error vector magnitude (EVM), output power exceeds 28dBm with associated drain efficiency of >20%. Additionally, noise performance is excellent for this device. From 1400 - 2000 MHz, the noise figure is <1.5dB for operation at V_{DS} = 28V and I_D = 50 mA.

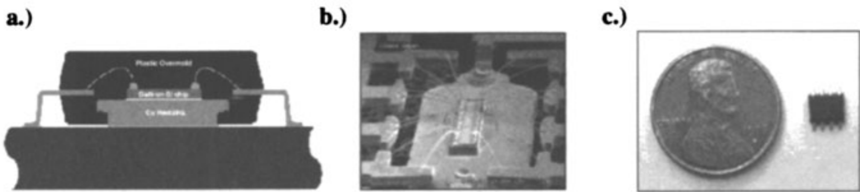

Figure 2. (a.) Cross-sectional schematic of SOIC package showing input and output leads, Cu heatsink, GaN-on-Si chip, and plastic overmold. (b.) GaN-on-Si device die bonded and wirebonded in SOIC package immediately prior to overmolding. The chip dimension is 1.65 mm × 0.55 mm. (c.) GaN-on-Si product in 8-pin SOIC package with size reference.

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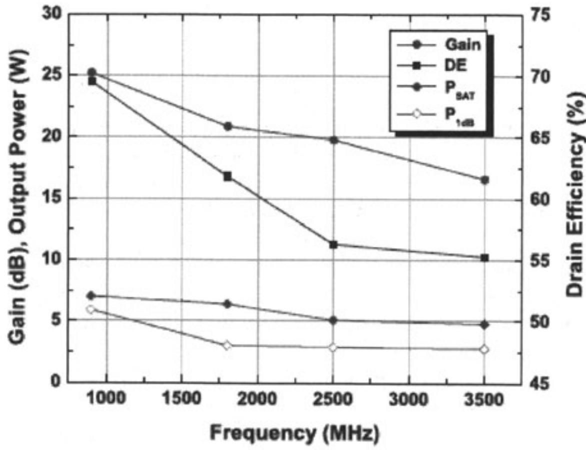

Figure 3. NPTB00004 CW performance summary across frequency from 900MHz to 3500MHz. Optimized source and load impedances were presented to the device at each frequency. $V_{DS} = 28V$.

Combining the high power density of GaN with the small footprint of an SOIC package, the recently-released NPT1004 delivers 45W of peak envelope power (PEP) at 2500 MHz. Producing 5W linear power, >13dB gain, and 27% drain efficiency at 2% EVM across the 2500 - 2700 MHz WiMAX band, this device is also an excellent general purpose 28V driver to a high power GaN final stage. Products with even higher output power in plastic packages are believed to be possible through thermal optimization including non-epoxy die attach.

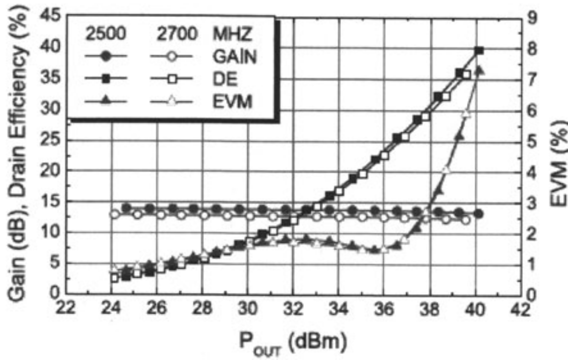

Figure 4. NPT1004 WiMAX performance across 200MHz bandwidth from 2500 - 2700 MHz. $V_{DS} = 28V$.

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HIGH POWER GaN-on-Si IN AIR CAVITY PACKAGES

28V Class

High power devices are assembled in traditional flange-based air cavity packages for excellent RF performance and improved thermal handling relative to plastic. Air cavity assembly of high power devices typically involves die attach with either AuSn or AuSi by eutectic formation. GaN-on-Si is the only GaN platform able to leverage the well-established AuSi eutectic process used by other power FET technologies such as Si LDMOS. For AuSi eutectic attach, the GaN-on-Si chip with backside Au electroplating is scrubbed onto the flange under force at a temperature of ~400°C. The eutectic reaction proceeds very quickly and, when optimized, can produce <5% total voiding with a thin (few μm) bondline and excellent thermal properties.

The flagship in the family of 28V air cavity products is NPT25100, delivering 125W PEP with >60% drain efficiency at 2.5 GHz. Under 2.5 GHz single-carrier OFDM modulation and 10 MHz channel bandwidth, this device produces 10W linear power at 2.0% EVM with 16.5dB associated gain and 26% drain efficiency. The excellent bandwidth of the technology enables the same product to operate at UMTS band from 2.11 - 2.17 GHz, producing >20W average power at an adjacent channel power ratio (ACPR) of -35 dBc. This performance across both UMTS and WiMAX bands is attributable to the low inherent output capacitance and high output impedance (Z_{OUT}) of GaN HEMTs relative to comparably-sized LDMOS FETs. These properties obviate the need for add ional L-C matching components such as MOS capacitor chips in the output network formed inside the package. Such components tend to reduce native bandwidth available from the FET chip in order to obtain impedances that can be easily matched by external circuitry. Representative W-CDMA sweeps of NPT25100 from 2110 - 2170 MHz are given in Figure 5. A 2500 – 2700 MHz Doherty power amplifier has also been designed and fabricated using two NPT25100 devices. Utilizing digital pre-distortion (DPD) linearization techniques, the GaN-on-Si Doherty PA with single carrier 10 MHz OFDM signal produced 20W output power across the 200MHz bandwidth with 33% drain efficiency, >11dB gain, <2% EVM, and excellent return loss. EVM was improved by ~1.5% (absolute) through use of DPD.

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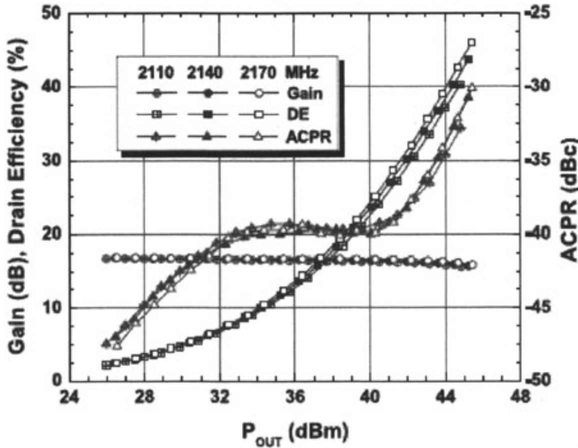

Figure 5. Typical NPT25100 W-CDMA performance in load pull system. V_{DS} = 28V.

48V Class

Thermal design must be carefully considered when optimizing GaN devices for high voltage and high power. Without appropriate thermal management at both the chip and package level, the high power density of GaN can cause performance degradation and/or fundamental limitations in device safe operating area. Thermal optimization at the chip level can be attained through device layout and through aggressive thinning. Improvement to the thermal properties of the package are also critical in order to maximize the power and efficiency available from the GaN-on-Si HEMT. All of these techniques have been employed to develop a family of 48V GaN-on-Si broadband transistors delivering power levels from 40W to 200W in a compact package. In the highest power case, package-level "power density" (defined as peak output power divided by package volume) reaches ~650 W/cm^3.

Chip-level optimization began with modification of the FET layout. In traditional, bar-style power FET geometries, gate contacts act as line sources of heat. Thermal coupling between adjacent gates can elevate peak junction temperature. A FET layout was designed and constructed to minimize this coupling by separating unit cells of 2mm gate width into a staggered or 'tiled' configuration. This significantly reduced thermal coupling and resulted in thermal improvements summarized in Figure 6. In this figure, a constant DC dissipated power was applied and peak temperature was measured using infrared imaging. Peak temperature of the optimized layout shown in 6(b.) is 25°C lower than for 6(a.) at the same dissipated power, leading to a 25% reduction in thermal impedance (R_{TH}).

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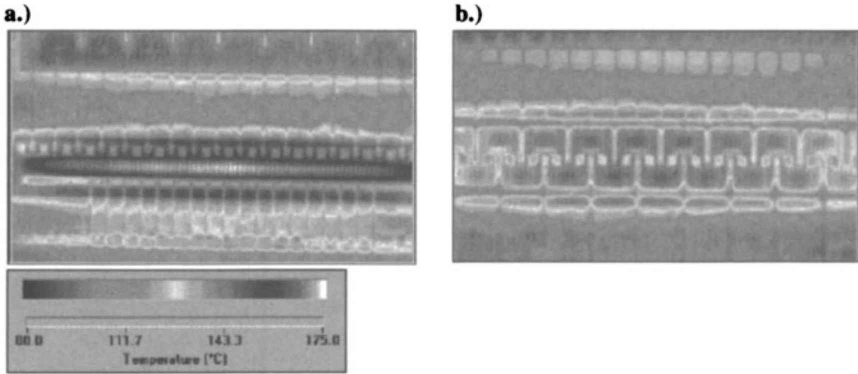

Figure 6. Infrared imaging shows difference in peak junction temperature of (a.) standard, bar-style FET layout and (b.) thermally-enhanced layout.

In addition to the layout modifications, more aggressive wafer thinning was employed to further reduce R_{TH}. Initial products launched at 28V employed thinning to 6 mils. Thermally-enhanced 28V products such as NPT25100 decreased substrate thickness to 4 mils. At this thickness, 48V devices with optimized layout produce a normalized thermal impedance of ~35°C-mm/W (R_{TH} multiplied by FET total gate width). Thinning to 2 mils produces an additional 15% reduction in R_{TH} to near 30°C-mm/W. These values compare favorably to GaN-on-SiC results, clearly demonstrating that thermal properties of Si (as compared to SiC) will not limit or preclude realization of high power GaN-on-Si FETs.

Optimization of packaging materials is also critical for thermal design. Thermal impedance from substrate to package can be comparable to R_{TH} from junction to substrate, underscoring the importance of the package for any high power device technology. For 48V GaN-on-Si, novel Cu-flanged air cavity packages were developed and implemented. Integration of Cu as a heat sink presents 2 main challenges: (1) the CTE of Cu precludes the use of conventional Al_2O_3 ceramic materials as package dielectric; and (2) the CTE mismatch between Cu and Si – combined with the ductility of Cu – can cause package bowing during assembly. Item #1 was addressed by package supplier(s) through development of organic materials with suitable dielectric properties and thermal expansion closely matched to Cu. Most of these organic materials cannot withstand AuSi eutectic die attach temperatures, so AuSn eutectic attach is currently used for all devices packaged in Cu. Item #2 is mitigated by optimizing thickness and/or pre-bow (intentionally bowing the package prior to assembly so it becomes flat post-assembly). This is a multivariate problem involving chip size and thickness, flange size and thickness, # of components, die attach method, and even lid attach conditions. These materials challenges were successfully addressed and enabled packaging and product development of high-power 48V GaN-on-Si devices.

Devices ranging in output power from 40W to 200W are currently in product qualification. These devices employ the epi and device fabrications details described earlier in conjunction with thermal improvements in layout, thinning, and packaging. A

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