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Editors: Martin Gall, Alfred Grill, Francesca Iacopi, Junichi Koike and Takamasa Usui

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Prefaceix

Materials Research Society Symposium Proceedings.....x

LOW-k DIELECTRICS I

**Effect of Trapping on Dielectric Conduction Mechanisms
of ULK/Cu Interconnects.....3**
Virginie Verriere, Cyril Guedj, David Roy,
Serge Blonkowski, and Alain Sylvestre

**Dual Damascene Reactive Ion Etch Polymer Characterization
Through X-ray Photoelectron Spectroscopy for 65 nm and
45 nm Technology Nodes.....11**
Samuel Choi, Leo Tai, and Chet Dziobkowski

**Interaction of O and H Atoms with Low-k SiOCH Films
Pretreated in He Plasma.....17**
O.V. Braginsky, A.S. Kovalev, D.V. Lopaev,
Y.A. Mankelevich, T.V. Rakhimova, E.M. Malykhin,
O.V. Proshina, A.T. Rakhimov, A.N. Vasilieva,
D.G. Voloshin, S.M. Zyryanov, and Mikhail R. Baklanov

**Characterization of Plasma Damage in Low-k Films by
TVS Measurements23**
Ivan Ciofi, Mikhail R. Baklanov, Giovanni Calbo,
Zsolt Tökei, and Gerald Beyer

LOW-k DIELECTRICS II

**Effects of Polymer Material Variations on High Frequency
Dielectric Properties31**
Gregory Pawlikowski

**Optimization of Low-k UV Curing: Effect of Wavelength on
Critical Properties of the Dielectric.....39**
German Aksenov, Patrick Verdonck, David DeRoest,
F.N. Dultsev, Premysl Marsik, Denis Shamiryan,
H. Arai, N. Takamure, and Mikhail R. Baklanov

**Application of UV Irradiation in Removal of Post-Etch
193 nm Photoresist.....45**
Quoc Toan Le, Els Kesters, L. Prager, Marcel Lux,
P. Marsik, and Guy Vereecke

POSTER SESSION: INTERCONNECTS

**Effects of Silica Sources on Nanoporous Organosilicate
Films Templated with Tetraalkylammonium Cations.....53**
Salvador Eslava, Jone Urrutia, Abheesh N. Busawon,
Mikhail R. Baklanov, Francesca Iacopi, Karen Maex,
Christine E. Kirschhock, and Johan A. Martens

**Electrical and Structural Properties of Ultrathin Polycrystalline
and Epitaxial TiN Films Grown by Reactive dc Magnetron
Sputtering.....59**
Fridrik Magnus, Arni S. Ingason, Sveinn Olafsson, and
Jon T. Gudmundsson

**A Study of Diffusion Barrier Characteristics of Electroless
Co(W,P) Layers to Lead-Free SnAgCu Solder65**
Hung-Chun Pan and Tsung-Eong Hsieh

METALLIZATION I

**Atomic Layer Deposition of Ruthenium Films on Hydrogen
Terminated Silicon.....73**
Sun Kyung Park, K. Roodenko, Yves J. Chabal,
L. Wielunski, R. Kanjolia, J. Anthis, R. Odedra,
and N. Boag

**Coupled Finite Element — Potts Model Simulations of
Grain Growth in Copper Interconnects.....79**
Bala Radhakrishnan and Gorti Sarma

**Electroless Cu Deposition on Self-Assembled Monolayer
Alternative Barriers.....85**
Silvia Armini and Arantxa Maestre Caro

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Frontmatter
[More information](#)

Rutherford Backscattering Spectrometry Analysis of Growth Rate and Activation Energy for Self-Formed Ti-Rich Interface Layers in Cu(Ti)/Low-k Samples93
Kazuyuki Kohama, Kazuhiro Ito, Kenichi Mori, Kazuyoshi Maekawa, Yasuharu Shirai, and Masanori Murakami

Adhesion and Cu Diffusion Barrier Properties of a MnO_x Barrier Layer Formed with Thermal MOCVD99
Koji Neishi, Vijay K. Dixit, S. Aki, Junichi Koike, K. Matsumoto, H. Sato, H. Itoh, and S. Hosaka

Electronic Transport Properties of Cu/MnO_x/SiO₂/p-Si MOS Devices105
Vijay K. Dixit, Koji Neishi, and Junichi Koike

METALLIZATION II

Stress Gradients Observed in Cu Thin Films Induced by Capping Layers.....113
Conal E. Murray, Paul R. Besser, Christian Witt, and Jean L. Jordan-Sweet

RELIABILITY

*** Large-Scale Electromigration Statistics for Cu Interconnects.....121**
Meike Hauschildt, Martin Gall, and Richard Hernandez

Effect of Dielectric Capping Layer on TDDB Lifetime of Copper Interconnects in SiOF133
Jeff Gambino, Fen Chen, Steve Mongeon, Phil Pokrinchak, John He, Tom C. Lee, Mike Shinosky, and Dave Mosher

EMERGING INTERCONNECT TECHNOLOGIES

Direct Metal Nano-Patterning Using Embossed Solid Electrolyte141
Anil Kumar, Keng Hsu, Kyle Jacobs, Placid Ferreira, and Nicholas Fang

*Invited Paper

Cambridge University Press
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Frontmatter
[More information](#)

**JOINT SESSION:
INTERCONNECT AND PACKAGING**

Low Temperature Direct Cu-Cu Immersion Bonding for 3D Integration	149
Rahul Agarwal and Wouter Ruythooren	
Failure Analysis and Process Improvement for Through Silicon Via Interconnects.....	155
Bivragh Majeed, Marc Van Cauwenberghe, Deniz S. Tezcan, and Philippe Soussan	
Effects of Thinned Multi-Stacked Wafer Thickness on Stress Distribution in the Wafer-on-a-Wafer (WOW) Structure.....	163
Hideki Kitada, Nobuyuki Maeda, Koji Fujimoto, Tomoji Nakamura, Kousuke Suzuki, and Takayuki Ohba	
* Power Delivery, Signaling and Cooling for 3D Integrated Systems	169
Muhannad Bakir and Gang Huang	
Copper Deposition Technology for Thru Silicon Via Formation Using Supercritical Carbon Dioxide Fluids Using a Flow-Type Reaction System.....	181
Masahiro Matsubara and Eiichi Kondoh	
Author Index.....	187
Subject Index.....	189

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978-1-107-40831-9 - Materials, Processes, and Reliability for Advanced Interconnects for Micro- and Nanoelectronics — 2009: Materials Research Society Symposium Proceedings: Volume 1156

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Frontmatter

[More information](#)

PREFACE

The semiconductor industry continues to follow Moore's law into 32 nm and 22 nm technologies, enabled by the development and introduction of new materials. Advanced interconnect structures require the use of porous dielectrics with further reduced k-values and even weaker mechanical properties, as well as much thinner metallization liners. In addition, the increasing resistivity of Cu with decreasing dimensions needs to be addressed in order to maintain the performance of the continuously shrinking devices. Innovations in materials, processes and architectures are needed to address these issues and to maintain the reliability of the interconnects.

Symposium D, "Materials, Processes, and Reliability for Advanced Interconnects for Micro- and Nanoelectronics — 2009," held April 14–17 at the 2009 MRS Spring Meeting in San Francisco, California, aimed to provide a forum for researchers around the world to exchange the latest advances in materials, processes, integration and reliability in advanced interconnects and packaging, and to discuss interconnects for emerging technologies, including 3D chip stacking and molecular electronics. A joint session was held with Symposium F, "Packaging, Chip-Package Interactions and Solder Materials Challenges."

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Martin Gall
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Frontmatter

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