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Ultra-Low Energy Ion Implantation of Si Into HfO_2-Based Layers for Non Volatile Memory Applications

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ABSTRACT

The fabrication of NCs is carried out using an innovative method, ultra-low energy (≤5 keV) ion implantation (ULE-II) into thin (6-9 nm) HfO_2–based layers in order to form after subsequent annealing a controlled 2D array of Si NCs. The implantation of Si into HfO_2 leads to the formation of SiO_2–rich regions at the projected range due to the oxidation of the implanted Si atoms. This anomalous oxidation that takes place at room temperature is mainly due to humidity penetration in damaged layers. Different solutions are investigated here in order to avoid this oxidation process and stabilize the Si-phase. Finally, unexpected structures as HfO_2 NCs embedded with SiO_2 matrix are obtained and show interesting memory characteristics. Interestingly, a large memory window of 1.18 V has been achieved at relatively low sweeping voltage of ± 6 V for these samples, indicating their utility for low operating voltage memory device.

INTRODUCTION

Nanocrystal memory (NCM) devices are competitive candidates for extending further the scalability of Flash-type memories [1-3]. Various process/materials alternatives have been suggested recently to establish a proven NCM technology in the timeframe required by the industry roadmap. In this direction, the fabrication of NCs into high-k dielectric matrices instead of SiO_2 materials has retained particular attention for achieving NCMs with low programming voltages and improved data retention. Indeed, a dielectric with a higher dielectric constant allows, in principle, to use a thicker tunnel oxide reducing leakage currents and, because of the smaller conduction band offset between the high-k film and the silicon substrate, to achieve the goal of a low voltage non-volatile memory device.
Among the different high-k materials under investigation, HfO_2 and their alloys are probably the most widely studied and are considered as very promising candidates for the integration in ultra-scaled commercial devices. Most of the data reported in literature on the synthesis of metallic and semiconducting nanocrystals for memory device application focus on the possibility to integrate the nanocrystals in these materials. Very few data are available on the synthesis of Si nanocrystals in a high-k matrix, especially in Hafnium oxide alloys. Superior programming efficiency and data retention characteristics have been obtained for systems described by Si nanocrystals deposited on HfO_2 films by LPCVD with SiH_4 at 600°C followed by in-situ HfO_2 deposition of the control dielectric [4-5]. Promising device results using Si or Ge NCs embedded in HfO_2 or HfAlO gate dielectrics have been recently presented [6-7]. Nevertheless, the fabrication of semiconducting NCs in high-k materials remains not straightforward. The main problems in terms of material science related to the use of a matrix

other than SiO_2 for the fabrication of memories are identified in ref. [8], and mainly concern the diffusion and oxidation of Si in high-k (HfO_2 and Al_2O_3) matrix.
Recently, we have extensively used ultra-low energy ion implantation (ULE-II) to synthesize single planes of Si nanocrystals embedded in very thin (5 to 10 nm) oxide layers. The depth-location of these two-dimensional (2D) arrays of particles below the wafer surface can be controlled with nanometer precision by tuning the implantation energy while their size and density can be controlled by varying the dose and annealing conditions [9]. These parameters were finally optimized to fabricate non volatile memory devices of improved characteristics [3]. In this paper, we extend this approach to synthesize a plane of Si NCs within high-k dielectrics. In particular, we present an approach to face the challenge of Si NCs formation into very thin (5-10 nm) HfO_2-based layers. This approach relates to the fabrication by ultra-low energy ion-beam-synthesis (ULE-IBS) of Si NCs in HfO_2 and HfSiO layers deposited by MOCVD on Si wafers. After implantation, all samples are annealed at high temperature for the purpose of NCs formation. Structural and chemical studies are carried out at the atomic scale by High Resolution Transmission Electron Microscopy (HREM) and Electron Energy Loss Spectroscopy in scanning mode by using a nanometer probe (STEM-EELS). The structural study reveals the oxidation of most of the implanted Si in the HfO_2-based layers while Si NCs are formed in the interfacial SiO_2 layer. Different strategies are tested in order to limit this oxidation including NH_3 annealing, implantation through thin Si_3N_4 capping layers and N and Si co-implantation in HfO_2 based layers. Unexpected structures as HfO_2 NCs embedded with SiO_2 matrix are obtained in addition to Si NCs in the SiO_2 interfacial layer (IL). In this case, capacitance-to-voltage characteristics of the MIS capacitors with NCs revealed strong hysteresis in terms of flat-band voltage shift after application of gate-voltage round-sweeps. These results suggest charge trapping and storage related to the formation of the NCs through the implanted/annealed high-k layers.

EXPERIMENT

As-deposited HfO_2 and HfSiO layers have been grown by MOCVD and are both nanocrystalline with very small grains of 2 nm. They are respectively 7 and 6 nm thick and are separated from the substrate by a very thin SiO_2 IL of 1 nm thick (not shown). Si+ has been implanted at low energy and high doses in these layers. The implantation energy has been chosen by running TRIM simulations [10] such as the projected range of the implanted Si is located in the middle of the high-k layer. The dose is higher than the nucleation threshold for the system Si/SiO_2 corresponding to 10 at.% [3] but lower than the threshold value for strong interface mixing effects [9]. For each layer, the implantation conditions are summarized in Table 1. On some HfO_2 layers, an additional 5 nm-thick layer of Si_3N_4 was deposited by electron cyclotron resonance-chemical vapor deposition (ECR-CVD) before implantation in order to prevent the Si oxidation. The samples have been further annealed at 1000°C for 30s under N_2 ambient for the purpose of Si-NCs formation except one which has been annealed under NH_3 at 950°C for 10 minutes.
The resulting structures were examined by High Resolution Transmission Electron Microscopy (HRTEM) in cross-section (XS) preparation to evidence the phase separation, as well as to determine the crystallographic nature of the NCs and the degree of crystallization of the surrounding matrix. Chemical images are performed by Energy Filtered TEM (EFTEM) and Electron Energy Loss Spectroscopy (EELS) with a probe of 1 nm used in scanning mode (STEM-EELS) to analyze the composition of the different layers. For this study, the cross-section samples were prepared for TEM observations using the standard procedure involving mechanical polishing and ion milling. Images were taken using a field emission TEM, FEI Tecnai™ F20 microscope operating at 200 kV, equipped with a spherical aberration corrector

and the last generation of the Gatan imaging filter series, the TRIDIEM. The spherical aberration corrector allows high quality HREM images with an increased signal/noise ratio and nearly no delocalization effect.
Prior to electrical measurement, 100 nm Al gate electrodes having a diameter of ~ 0.75 mm were thermally evaporated into the samples through a shadow mask. For ohmic contact, gold was evaporated on the back side of Si substrates. High frequency capacitance-voltage (C-V) measurements of metal-insulator-semiconductor (MIS) structures were carried out using a HP4192A impedance analyzer. Post-metallization annealing of all the MIS structures were carried out at 400°C for 20 minutes in forming gas prior to measurement. Control MIS structures of the gate dielectrics without undergoing the implantation step were also fabricated using the same processes as the implanted samples and examined for comparison purposes.

film	thickness (nm)	grain size (nm)	implant	energy (keV)	dose (x10^{16} at.cm^{-2})	annealing conditions
HfO_2	7	2 nm	Si	3	1.5	1000°C 30s N_2
HfO_2	9	4 nm	Si	5	1.5	1000°C 30s N_2
HfO_2	7	2 nm	N+N+Si	1+2.5+3	0.3+0.7+1.5	1000°C 30s N_2
HfO_2	9	4 nm	N+N+Si	1+3+5	0.2+1.0+1.5	1000°C 30s N_2
HfO_2+Si_3N_4	7+5	2 nm	Si	8	1.5	1000°C 30s N_2
HfO_2+Si_3N_4	9+5	4 nm	Si	9	2	1000°C 30s N_2
HfO_2	7	2 nm	Si	3	1.5	950°C 10min NH_3
HfO_2	9	4 nm	Si	5	1.5	950°C 10min NH_3
HfSiO	6	2 nm	Si	2	1	1000°C 30s N_2

Table 1: implantation and annealing conditions of the films discussed in this work.

RESULTS AND DISCUSSION

Fig. 1(a) shows a Bright Field XS-TEM image of the HfO_2 layer after Si+ implantation and subsequent annealing. The SiO_2 interfacial layer (IL) separating the HfO_2 layer and the Si substrate is 7.2 nm instead of 1.2 nm for the as-deposited layer. The HfO_2 layer, in dark contrast, is now polycrystalline (see HREM image in Fig. 1b) with nanograins of 4 nm in diameter. The high-k layer is 10.9 nm thick i. e., has encompassed a swelling of 4 nm comparing to the as-deposited layer. Regions with clear contrast, very similar to the one in the IL, are visible in the high-k layer. They are amorphous (see Fig. 1b), Si-rich and separate the HfO_2 grains.

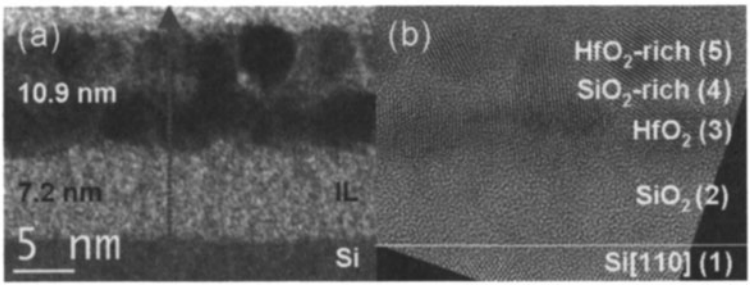

Fig. 1: (a) BF and (b) HREM images of the HfO_2 layer implanted with Si+ at 3 keV for a Si excess of 26 at. %. The HfO_2 grains are separated by amorphous Si rich regions. The red arrow corresponds to the line scanned across the film for the STEM-EELS acquisition.

STEM-EELS analyses have been performed in order to examine the different EELS signatures in the low-energy loss domain and around the core Si-K edge in order to identify the corresponding phases. The experiment consists in scanning a small probe 1 nm in diameter across the interface with the Si substrate going towards the film. An EELS spectrum is recorded at each position of the probe along the line. The analysis in the core-loss region (Hf-M and Si-K) shows that both the IL and the clear regions separating the HfO_2 grains are SiO_2-rich (Fig. 2a) while from the low-loss analysis, beyond the signatures of the Si substrate, the SiO_2 IL and the HfO_2-based nanocrystals, a signature characteristic of the plasmon of Si has been detected in addition to the one of the SiO_2 IL layer (Fig. 2b).

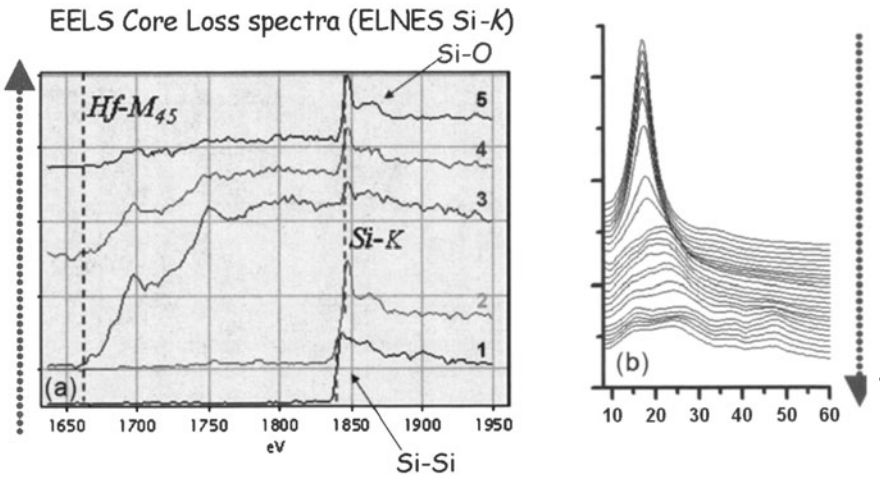

Fig. 2: STEM-EELS analyses (line-spectrum) of the different regions as indicated by the arrow on Fig. 1(a), (a) in the core-loss region and (b) in the low-loss region. The number in (a) correspond to the area defined in Fig. 1b.

In order to localize within the film where are located the different phases identified by STEM-EELS, EFTEM chemical images have been performed. The images are formed with the electrons that are selected by a slit with a width of +/-2 eV placed in the energy-dispersive plane of the spectrometer at an energy position of 17 eV, 23 eV and 47 eV respectively, corresponding to the Si and SiO_2 plasmon peak positions for the formers and a strong contribution of the Hf-*O23* edge in HfO_2 for the last one. Isolated grains of HfO_2 with white contrast are revealed with 47 eV energy filtering (Fig. 3c). The SiO_2-rich (SiO_x) areas like the IL and regions between the HfO_2 grains can be recognized by 23 eV energy filtering (Fig. 3b). The EFTEM at 17 eV is very interesting, showing no visible contrast in the HfO_2 region but Si NPs in the IL (Fig. 3a). These NPs, with a diameter of 1-2 nm, are located in a 3 nm-thick region at 1.5 nm from the Si substrate and 3 nm from the first HfO_2 NCs.

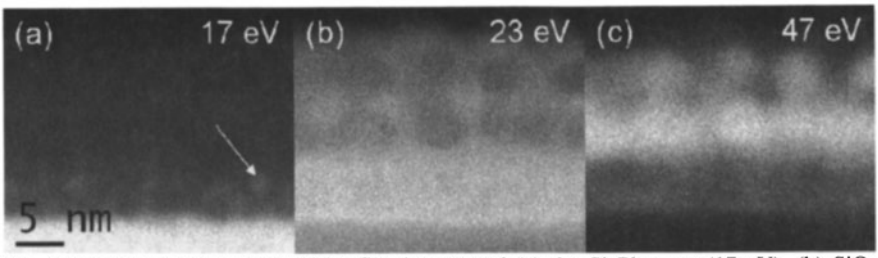

Fig. 3: EFTEM images obtained by filtering around (a) the Si Plasmon (17 eV), (b) SiO_2 plasmon (23 eV) and (c) strong contribution of Hf-*O23* (47 eV).

As a consequence, one can conclude that the majority of the Si implanted in the HfO_2 region has been oxidised, giving rise to the separation of the HfO_2 grains. The swelling measured for the high-k layer after implantation and annealing is 4 nm, i.e. larger than the 3 nm expected for only matter addition of the total dose. This is in good agreement with the partial oxidation of the implanted Si, the dramatic swelling of the IL (expansion of 6 nm after implantation and annealing) being then due to the oxidation of the Si substrate. This oxidation of the Si implanted in the HfO_2 layer already takes place before annealing (not shown). During annealing, part of the implanted Si diffuses in the SiO_2-IL and precipitates to form Si NCs.

The oxidation of implanted Si has been studied in detail when implanted in very thin SiO_2 matrix [10-13]. This so-called "anomalous" diffusion takes place before any annealing, immediately after implantation because the heavily damaged SiO_2 layers absorb humidity. These water molecules are driven in the layers, dissociate and finally react with the implanted Si to form SiO_2. During annealing, further dissociation of OH takes place and finally most of the H atoms diffuse out to the surface. The penetration and final concentration of water molecules do not depend on the relative humidity in the atmosphere but are only limited by the degree of damage i. e., by the concentration of defects, in the SiO_2 matrix. In the case of Si implanted in SiO_2, we have evaluated that 40% of the implanted Si is oxidised. The remaining Si precipitates to form Si NCs. In the case of HfO_2, it seems that the oxidation is even more efficient probably due to the hygroscopic nature of the high-k layers [14] and the presence in the layer itself, after deposition, of OH groups in the layer.

Different strategies have been tested in order to avoid or limit this anomalous oxidation. The first one consists in co-implanting N in the HfO_2 layer in order to trap the oxygen atoms. For this, two N profiles have been implanted at very low energy, 1 and 2.5 keV with doses corresponding to 15 at.%. Higher N content would deteriorate the electrical properties [15]. The Si has been implanted at 3 keV with Si excess corresponding to 25 at.% as previously. We observe after annealing in the same conditions the formation of the same structure as previously, with amorphous white regions in the HfO_2 layer. The comparison of zero-loss EFTEM images with the same mean thickness as measured on the associated thickness map shows that these Si rich amorphous regions are present in lower proportion in the layer containing N (not shown). EFTEM image obtained by filtering at 23 eV (SiO_2 plasmon, see Fig. 4d) confirm that this region as well as the IL are SiO_2 made. These SiO_2 regions in the HfO_2 layer are again already present in the as-implanted sample. Furthermore, STEM-EELS experiments have shown that N is located near the Si substrate, in the SiO_2 IL (not shown). During annealing N has diffused from the film into the SiO_2 IL.

The IL is now 5.5 nm instead of 7.2 nm for the sample implanted with Si only, evidencing a lower oxidation of the Si substrate. A layer of NPs is now clearly visible in the BF images within the SiO_2 IL layer (see Fig. 4a). These particles are crystalline as we can see in the HREM image of Fig. 4b showing interplanar distances of 0.31 nm, which corresponds either

to Si or monoclinic HfO_2 (111) planes. EFTEM images at 17 eV (see Fig. 4c) confirm that these particles are composed of Si. In conclusion, N co-implantation has limited the anomalous oxidation of the implanted Si. Nevertheless, the Si NPs are still not formed in the high-k layer but again within the SiO_2 IL.

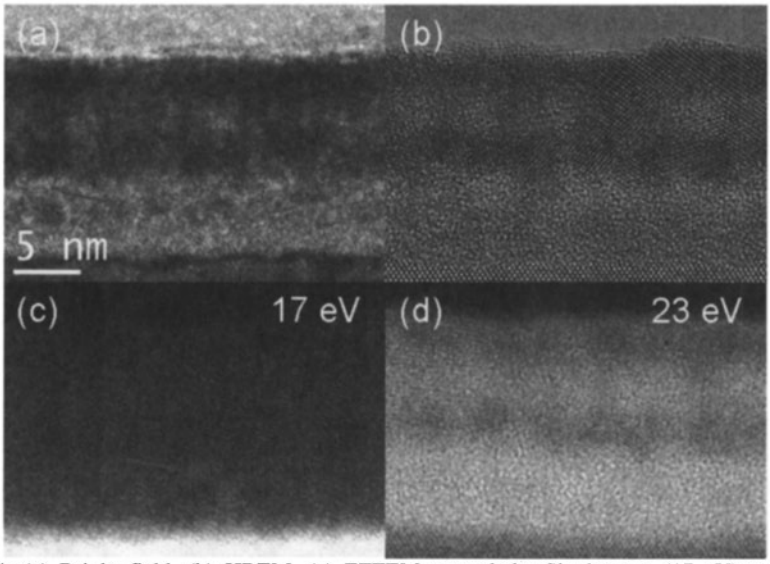

Fig. 4: (a) Bright field, (b) HREM, (c) EFTEM around the Si plasmon (17 eV) and (d) EFTEM around the SiO_2 plasmon (23 eV) for the N+Si implanted HfO_2 film.

The same strategy (N+Si implantation) has been used in thicker (9 nm) monoclinic HfO_2 layers as well has in 6 nm amorphous HfSiO layers, with the same result (oxidation of the Si remaining in the HfO_2 layer and formation after annealing of Si NCs within the IL layer). The annealing under NH_3 ambient instead of N_2 of Si implanted HfO_2 layers does not help in avoiding the Si oxidation, neither than the implantation through a SiN capping layer.

C-V measurements have been performed for the different implanted layers. The best memory window has been found when the anomalous oxidation of the Si implanted within HfO_2 leads to disconnected HfO_2 grains, aligned following 2 parallel layers (see Fig. 1b). In this case we have formed an unexpected structure made of HfO_2 quantum wells embedded within a SiO_2 insulating layer. Such a nanostructured layer (HfO_2 NCs within SiO_2) has already been fabricated by annealing HfSiO alloys under O_2 at high temperature and show nice electrical performances [16].

A third layer of discrete traps (Si NCs) is embedded in the SiO_2 IL separating the HfO_2 NCs from the Si substrate, giving rise to a third level NCs storage. In this case, significant hysteretic effect with a memory window (ΔV_{fb}) of 1.18 V is observed for sweeping voltages of ±6 V. It is noteworthy that effect of mobile ions on charge trapping can be ruled out, as no significant hysteresis has been observed in the control sample without any nanocrystal. The frequency dependent C-V curves were further measured in the range of 1 MHz to 50 kHz (not shown). Little frequency dispersion has been observed in the depletion region confirming that the charge storage was rather in NCs rather than in defect sites. All the samples show clockwise hysteresis indicating the movement of a net negative charge (electrons) in the dielectric layer. The most profound reason can be attributed to the electron injection from the

gate, when the device is biased at accumulation, and subsequent trapping in the dielectric coating NCs. Further charge retention measurements are under process.

This unexpected but interesting structure will be optimised by the deposition of a control oxide in order to limit the charge leakages to the gate. Annealing under O_2 ambient could be used in order to better control the oxidation process as in ref. [16] and therefore the size and density of the HfO_2 NCs. Finally, HfO_2 layers are interesting for NCs memories mainly for their improved electrical characteristics when used as tunnel oxide. As a consequence, multilayers structures, composed of HfO_2 layers on Si substrate, with on top SiN layers, will be implanted in the future, to get rise from the material science difficulties in stabilising a Si phase in such dielectric layers.

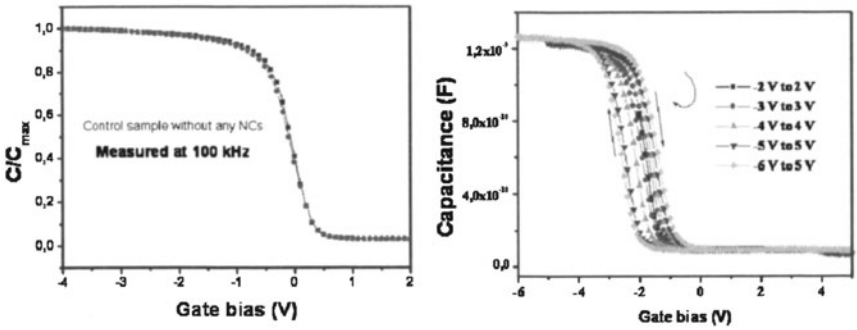

Fig. 5: High frequency capacitance-voltage (C-V) measurements of metal-insulator-semiconductor (MIS) structures for (a) the as-deposited HfO_2 layer and (b) the HfO_2 layer implanted with Si+ at 3 keV with an excess of 26 at.% and annealed at 1000°C for 30s.

CONCLUSION

The implantation of Si+ within HfO_2 based layers deposited by MOCVD on top of a Si substrate leads to the formation of Si NCs within the SiO_2 interfacial layer and to the oxidation of the Si implanted within the HfO_2 top layer. This anomalous oxidation of implanted Si in thin insulating layers is a well known process and is due to moisture penetration in the heavily damaged layers after ion implantation. Annealing under NH_3 ambient instead of N_2 has no detectable effect on the final structure and do not limit the oxidation extend. Nevertheless, this oxidation process is slightly reduced when co-implanting N before the Si implantation or when implanting through SiN capping layers. Finally, when the anomalous oxidation is the most efficient and leads to the clear separation of the HfO_2 grains, interesting memory characteristics are found.

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