Novel Devices

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Tunneling MOSFETs Based on III-V Staggered Heterojunctions

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ABSTRACT

A critical problem for the progression of CMOS electronics to the nanoscale is the reduction of power density, while at the same time preserving high speed performance. One of the most promising approaches is to aggressively reduce the power supply voltage by using a novel device, the tunneling MOSFET (TMOSFET), which is a MOSFET that operates by tunnel-injection of carriers from source to channel, rather than by conventional thermionic emission. TMOSFETs benefit from steep (sub-60mV/dec) gate turn-on characteristics. In this paper we show that TMOSFET designs based on staggered heterojunctions are particularly promising, since the choice of materials for the injector (source) and channel allows optimization of the tunneling probability at the heterojunction. Analysis and simulation of MOSFETs based on the GaAlSb / InGaAs material system are presented. The energy offset between the valence band of the injector and the conduction band of the channel at the heterojunction can be tailored over a wide range, from negative values ("offset" band lineup) to values in excess of 1eV. We find by simulation that for optimal values of effective heterojunction bandgap near 0.2eV, the resulting MOSFETs are capable of delivering >0.5mA/mm while maintaining on-off ratio greater than 10^4 over voltage swing of 0.3V. We also discuss a variety of materials-related challenges that must be overcome to realize the predicted performance. Among these are the need to provide near ideal heterojunctions between the materials, employ high K dielectrics with very low interface state density, and achieve good alignment between the gate and the heterojunction. Different configurations for the tunneling MOSFETs are presented.

INTRODUCTION

During decades of progress in CMOS electronics following Moore's law, the power dissipation per unit area has been kept within bounds by a progressive scaling of the power supply voltage V_{DD}. Further reduction in V_{DD}, however, is impeded by the finite sub-threshold slope associated with MOSFETs of conventional design. It is well-known that MOSFET drain current varies with gate voltage at best at a rate of 60 mV/decade at room temperature (and often more slowly) because the transistor operation relies on thermal excitation of carriers over an energy barrier (modulated by the gate voltage) between the source and the channel [1]. In order to maintain a low OFF current in a typical MOSFET, the threshold voltage cannot be lower than about 0.25-0.3 V. To achieve a useful ON current, a gate overdrive voltage of order 0.3-0.5 V is also required, dictating that values of V_{DD} for high performance applications cannot be decreased below 0.6-0.8V. Since power dissipation due to switching energy is proportional to $C_{eff} V_{DD}^2 f_{clk}$, where C_{eff} is an effective load capacitance and f_{clk} is the clock frequency, it is difficult to avoid increasing power density per unit area as gate dielectrics shrink and f_{clk} increases.

An approach to addressing the power dissipation problem has recently received considerable attention, based on Tunneling MOSFETs [2-9] (abbreviated here as TMOSFETs). These devices are expected to attain sub-threshold swings considerably better than conventional MOSFETs, down to the 20 mV/decade region, as shown in Fig. 1. As a result, it can be anticipated that power supply voltages for CMOS electronics could be reduced to values as low as 0.2-0.25V while still maintaining high speed performance. In order to achieve this goal, the TMOSFETs should, in addition to the sub-threshold swing metric, achieve low values of OFF current (of order 10-100 nA/um of gate width) and high values of ON current (of order 1mA/um of gate width).

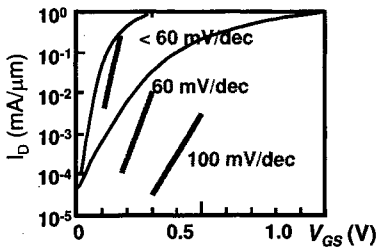

Figure 1: Schematic Id-V_{GS} characteristics of present-day MOSFETs, and those of proposed TMOSFETs.

The fundamental operating principle of the TMOSFET is to provide current from the source to the channel by a tunneling process rather than by thermionic injection. This permits the output current to be independent of KT, and thus avoids the 60 mV/decade constraint. Figure 2 compares the schematic band diagram of a conventional MOSFET and that of the TMOSFET under operating conditions. Carriers tunnel between the valence band of the source and the conduction band of the channel (for an n-channel device).

One of the critical considerations for the implementation of high performance TMOSFETs is to attain high tunneling probability for carriers. There are a variety of on-going efforts to fabricate TMOSFETs with Si materials [2-5,8]. The high energy gap - which provides the barrier to tunneling between- source and channel- tends to decrease the tunneling probability and thus reduce

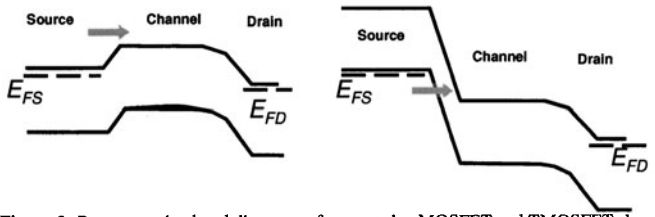

Figure 2: Representative band diagrams of present-day MOSFET and TMOSFET showing different injection mechanisms from source to channel.

the ON current of the device. A preferable approach is to employ a heterojunction between source and channel - that is, employ different materials for these two regions - and to choose the materials so that their band alignment involves a staggered configuration [5-7].

The set of III-V semiconductors provides a rich array of bandgaps and band lineups that can be exploited to make heterojunctions of different characteristics. Figure 3 shows pictorially the band lineups of some familiar binary and ternary III-V materials (although not all are lattice-matched). In order to achieve a high tunneling probability, a choice of materials that involves a small interface bandgap is appropriate, typified by the lineup between InGaAs and GaAlSb. The tunneling probability across such a heterojunction can be dramatically higher than for the case of Si. Figure 4 illustrates, for example, the tunneling current density expected on the basis of

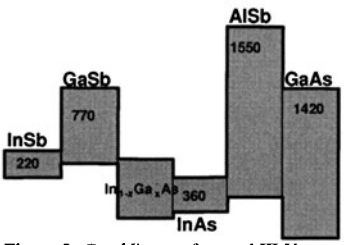

Figure 3: Band lineup of several III-V semiconductors.

simple Zener tunneling theory, for tunnel diodes prepared with Si and with a III-V semiconductor choice with interface bandgap (E_{int}) of 0.2eV. The considerable benefit of III-V semiconductor relative to Si is clear.

III-V MOSFET design entails a variety of considerations that differ from the Si case: 1) higher peak velocity and ballistic injection velocity; 2) reduced density of states, leading to lower current levels at a fixed fermi level vs Si ; 3) need for electrostatic confinement to shield the drain potential in small FETs, which is difficult to achieve with the larger wavefunction spread typical of III-Vs ; 4)"source starvation" in ballistic FETs, associated with the difficulty of maintaining thermal equilibrium in the source during ballistic current injection ; 5) oxide issues and interface characteristics. This paper describes numerical simulations of device characteristics, and tradeoffs in device design in relation to band offsets, doping levels, and gate geometry.

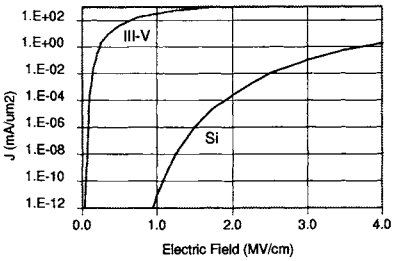

Figure 4: Tunneling current density computed for Si p-n junctrion and for III-V heterojunction with 0.2eV interface bandgap, using simple Zener theory.

TMOSFET STRUCTURE

The implementation of TMOSFETs using III-V materials can be done with several geometries such as the one shown schematically in Fig. 5a. The source consists of p-AlGaSb, which injects electrons into the channel of InGaAs (which is doped lightly p type or is undoped, so that the current flow without gate voltage applied is small). The drain is n+ InGaAs or other

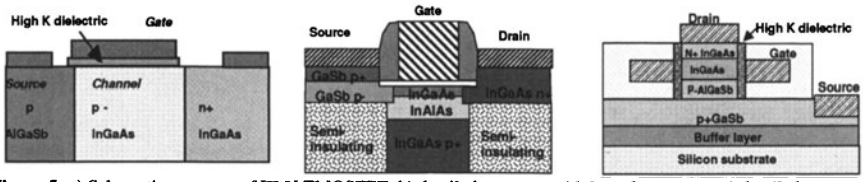

Figure 5: a) Schematic structure of III-V TMOSFET; b) detailed structure with lateral geometry; c) detailed structure in vertical embodiment.

material with potentially large bandgap. Practical implementations of this structure could be have both lateral or vertical geometries, as shown in figure 5b,c. The lateral geometry is fabricated using epitaxial regrowth for the source (and potentially the drain, as shown in the figure). A regrowth process for source/drain regions of III-V MOSFETs has already been demonstrated at UCSB [10]. The vertical structure can be mapped into a pillar or nanowire embodiment in which the gate is wrapped around the entire device.

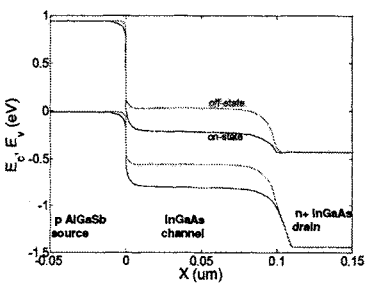

Figure 6: Simulated band diagram of n-channel TMOSFET between source and drain, under different VGS biases.

The band diagram between source and drain along the channel surface for a representative structure is shown in Fig. 6. Under control of the gate voltage, the band lineup between channel and source is varied between the condition where no tunneling can occur (OFF state) and the condition

where tunneling is permitted because of the overlap in energy of empty states from the channel conduction band and filled states of the source valence band.

The detailed choice of materials is subject to the constraint of approximately matching lattice constants to avoid misfit dislocation formation. Fortunately there is a rich set of materials including ternary and quaternary III-V compounds from which heterojunction combinations can be selected such that the thin layers needed for TMOSFETs are within the allowed critical thicknesses, or are even lattice-matched (for example, by choosing AlGaAsSb instead of AlGaSb [7]). The material bandgap and band offset estimates used in the design must account for the effects of strain as well as of quantum confinement of the carriers in the thin channel layer.

While figure 6 depicts an n-channel device, it is possible to implement similar structures for p-channel operation with the same material system.

TMOSFET CURRENT-VOLTAGE CHARACTERISTICS

To assess the performance of the TMOSFETs, we have carried out calculations employing 2D solution of current transport and Poisson equations, using the DESSIS software, taking into account direct band-to-band tunneling between source and channel. The tunneling current calculated within the DESSIS program has been shown to be in good accord with the results of a direct calculation based on a two-band model and the WKB approximation [6,7]. Resultant device characteristics are shown in figure 7 (for V_{DS}=0.3V). The turn-on characteristics show a sub-threshold slope comfortably below 60 mV/decade, and drain current of 0.5 mA/um of gate width is achieved at V_{GS}=0.3 V. The ON/OFF current ratio is 10^4-10^5. These characteristics are very favorable for future highly scaled CMOS circuits. The computed characteristics also exhibit leakage current for negative V_{GS} values, associated with tunneling current at the drain channel junction (which is dependent on the choice of material for the drain).

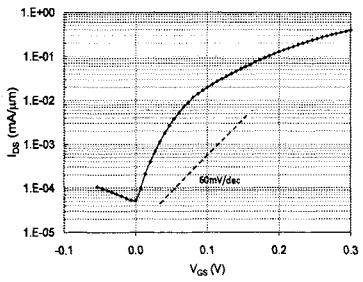

Figure 7: Id-Vgs characteristics of GaAlSb/InGaAs TMOSFETs simulated numerically as described in text.

MATERIALS AND FABICATION CHALLENGES

There are a variety of design issues critical to the performance of TMOSFETs. Well-established limits to the current per unit gate width of III-V MOSFETs are related to the velocity of carriers at the top of the source/channel barrier ("virtual source") and the density of carriers at that position, for a given applied gate voltage. The number of carriers attainable with III-V channels is

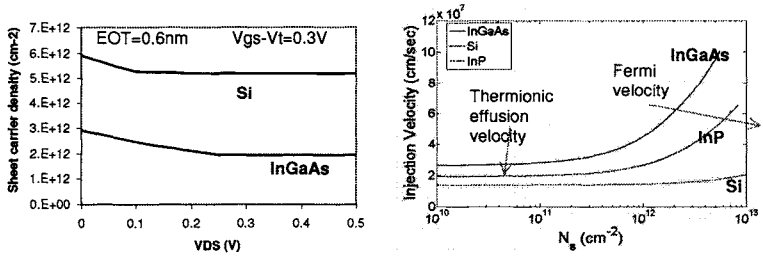

Figure 8: a) Computed density of electrons in the channel of conventional MOSFETs based on Si and on InGaAs at the virtual source, for a gate overdrive of 0.3V, and EOT of 0.6nm. b) Computed average velocity of electrons at the virtual source in conventional MOSFETs, as a function of density of carriers.

limited by the low density of states (DOS) for the conduction band of these materials. For example, figure 8a illustrates the computed channel charge density for Si and for n-$In_{0.53}Ga_{0.47}As$ channels vs drain voltage, for gate overdrive of 0.3V and equivalent oxide thickness (EOT) of 0.6nm. The factor of x2.5 advantage of Si is apparent, as a result of its higher DOS (in turn related to its higher electron effective mass as well as the degeneracy of the conduction band minima). The low effective mass of InGaAs, however, leads to higher velocity of carriers at the virtual source. At low gate overdrives this advantage follows the thermal velocity (square root of the m* ratio), as expected from Boltzmann statistics. However, at realistically high gate overdrive values, the velocity improvement of III-V semiconductors increases considerably as a result of band-filling and the resultant increase in the fermi velocity of carriers in the degenerate conduction band. The improvement in velocity of x4 over Si leads to an overall increase in the drain current expected for the III-V MOSFET embodiment, according this simple quasi-equilibrium picture. Additional considerations modify this picture, associated with the extent to which the states in the conduction band of the channel can be filled from the source [12]. These effects limit the drain current that can be conducted in traditional MOSFETs, for a given value of gate voltage, to values in the range of 1-2 mA/um for a gate overdrive of 0.3V. The drain current in a TMOSFET is strictly limited by this value, and will be smaller if the tunneling probability is not sufficiently high.

The OFF current of TMOSFETs (for V_{GS}=0V and V_{DS}=0.3V, for example) is related to carrier generation other than through tunneling at the channel/source junction, as shown in figure 9.

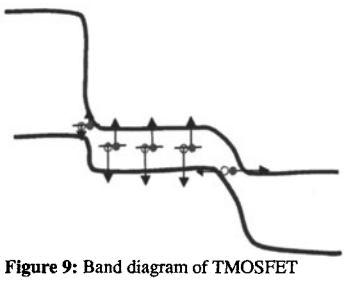

Figure 9: Band diagram of TMOSFET showing schematic carrier generation processes that can contribute to OFF current.

In TMOSFETs based on homojunctions, tunneling at the channel/drain junction also contributes to carrier generation. This component can be suppressed by choosing a material combination featuring an appropriately high interface bandgap at the drain/channel heterojunction. Additionally, electron-hole generation can occur within the channel itself (particularly if the material has a low bandgap) and at the source/channel interface. Since at this last position the interface energy gap is constrained to be low in order to achieve sufficiently high tunneling rates, the interfacial defect density must be minimized.

The implementation of MOSFETs with III-V semiconductors has been hampered for decades by the lack of a suitable oxide or dielectric featuring low interface state densities. Recent results have been very promising; GaAs/InGaAs MOSFETs have been demonstrated employing (Gd,Ga)oxide dielectrics and Al_2O_3 dielectrics, among others [13-15]. Interface states between channel and gate dielectric have two detrimental effects on TMOSFETs. One effect is to increase the rate of carrier generation at the interface between channel and source, which leads to an increase in leakage current in the OFF state, as described above. Another effect is to electrostatically shield the channel / source interface potential from the effects of the applied gate voltage. Figure 10 illustrates schematically the gate geometry for the TMOSFET. Capacitance C_{it} associated with the interface density of states D_{it} (with C_{it}=qD_{it}) shunts C_d, the geometric capacitance of the source/channel interface, thus leading to an increase in the value of V_{GS} required to achieve a specific surface channel potential change. Dielectrics with small equivalent oxide thickness values (EOT below about 1 nm) are required for proper operation of TMOSFETs. Smaller EOT values

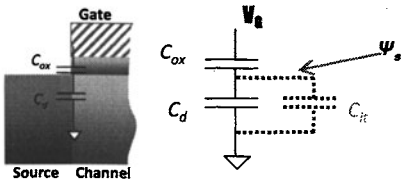

Figure 10: Schematic diagram showing components of input capacitance, and factors that determine the channel potential swing. The effect of interface states is shown.

will increase tolerance to presence of interface states. In order to achieve the proper capacitance ratios, it is also important to accurately align the gate with respect to the heterojunction.

An additional materials technology required to allow the TMOSFETs described here to be effective in large scale, high performance CMOS circuits is the deposition of appropriate III-V materials on large Si substrates with low defect density. Vast strides have been made in recent years in the associated growth technology [16].

CONCLUSIONS

TMOSFETs implemented with III-V semiconductors using staggered heterojunction band line-up have the potential to solve the critical power density challenge faced by emerging CMOS technology. TMOSFET operation may well become one of the most compelling reasons to pursue III-V materials for CMOS applications. There remain, however, numerous challenges in material and fabrication technology for the successful implementation of this technology.

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