Modeling Nanowire and Double-Gate Junctionless Field-Effect Transistors

Being the first book on the topic, this is a comprehensive introduction to the modeling and design of junctionless field-effect transistors. Beginning with a discussion of the advantages and limitations of the technology, the authors provide a thorough overview of published analytical models for double-gate and nanowire configurations, before offering a general introduction to the EPFL charge-based model of junctionless FETs. Important features are introduced gradually, including nanowire versus double-gate equivalence, technological design space, junctionless FET performances, short-channel effects, transcapacitances, asymmetric operation, thermal noise, interface traps, and the junction FET. Additional features compatible with biosensor applications are also discussed. This is a valuable resource for students and researchers looking to understand more about this new and fast-developing field.

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Foreword

Since its first publication in 2009, the junctionless transistor [1] proved to be a very popular device amongst semiconductor research groups worldwide. Junctionless transistors are very simple to manufacture and the junctionless architecture has been successfully applied to many semiconductor materials including single-crystal and polycrystalline silicon and germanium, III-V compounds, ZnO, Indium-tin oxide (ITO), transition metal dichalcogenides, etc.

Figure 0.1 shows the number of publications and citations in Web of Knowledge corresponding to the search word "junctionless transistor". Well over a hundred papers were published on junctionless transistors each year during 2009–16, with more than a thousand corresponding citations.

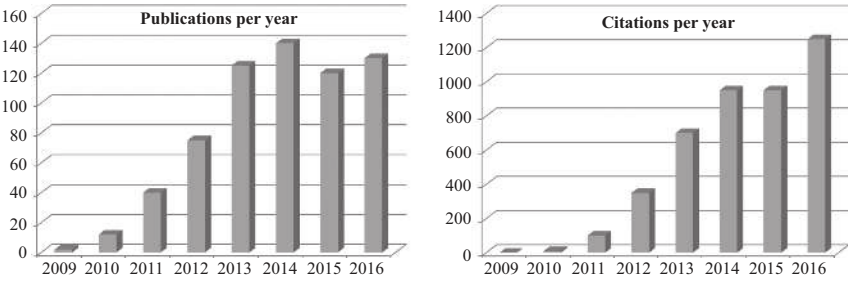

Figure 0.1 The number of publications (a) and citations (b) per year, corresponding to the search word "junctionless transistor" in Web of Knowledge.

Junctionless transistors are also increasingly being used as detectors such as gas, chemical, biochemical, and pH sensors [2, 3]. They are also being considered for the formation of low-thermal-budget active interconnects in future monolithic 3D integrated circuits [4].

Although the electrical characteristics of a junctionless transistor are quite similar to those of a conventional inversion-mode device, there are key differences in transport and capacitance properties: transport in a junctionless transistor is largely in the bulk of the semiconductor instead of in an inversion channel. As a result, surface scattering and trapping of carriers is reduced, which improves noise figure and allows one to make transistors in materials that have problematic interface properties, *n*-channel germanium MOSFETs being a good example.

Accurate modeling of the junctionless transistor is essential for comparing the performance of these devices with those of other types of transistors and for different types of applications. The publication of the book *Modeling Nanowire and Double-Gate Junctionless Field-Effect Transistors* by Doctors Farzan Jazaeri and Jean-Michel Sallese, two renown experts in the field, is thus timely and will bring valuable information to those interested in advanced device physics, simulation, and design.

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Preface

Metal-oxide semiconductor field-effect transistor scaling is following the prediction of the Moore's law enunciated in 1965 [5]. So far, this trend for miniaturization has never been invalided, enabling the industry of semiconductors to cope with the everlasting demand for higher performance at lower cost. However, this scaling becomes increasingly difficult to follow due to inherent process and device performance limitations for technology nodes beyond tents of nm. To stand the pace of downscaling, nonclassical device architectures have been continuously proposed in the ITRS roadmap.

The junctionless field-effect transistor is one of these nanoelectronics devices that is expected to withstand the downscaling of Complementary Metal-Oxide–Semiconductor (CMOS) technology by enabling easier fabrication processes, while allowing high performance. In addition, semiconductor nanowires largely used for label-free biosensing are essentially junctionless FETs without any gate.

Therefore, since the first implementation of junctionless FET nanowires by J. P. Colinge in 2009, growing interest in these devices in different fields of research motivated the authors to write a book dedicated to analytical modeling of double-gate and nanowire junctionless FETs. In contrast to the abundant literature on modeling and compact modeling of inversion-mode MOSFETs, analytical modeling of field-effect transistors without junctions is still following different strategies.

After discussing the advantages and limitations of junctionless field-effect transistors in the first introductory chapter, a thorough overview of published analytical models for double-gate and nanowires configurations is presented in Chapter 2, including the mains assumptions which are introduced.

In Chapter 3 and beyond, the analytical model of the so-called EPFL junctionless field-effect transistor is presented. After discussing the roots ending with a charge-based model valid in all the regions of operation, important features are introduced gradually in Chapters 4–13, each of which targets a specific feature. These topics include nanowire versus double-gate equivalence, technological design-space, junctionless FET performance, short-channel effects, transcapacitances, asymmetric operation, thermal noise, interface traps, and a revisited model for JFETs. In addition a general mobility extraction technique is proposed.

We suggest readers see Chapter 3 for a general introduction to the charge-based model before proceeding further. This is where the main ideas are introduced that will thus be used in the following chapters.

We hope this book will be useful to people interested in modeling these new types of field-effect transistors, which are likely to find diverse applications, not only in nanoelectronics, but also in a large variety of biosensors.

The authors would like to acknowledge Doctors Lucian Barbut and Didier Bouvet who actively participated in the research done at EPFL and also Doctors Maria-Anna Chalkiadaki, Wladek Grabinski, and Professor Christian Enz who provided invaluable support. Many thanks to Professors Christophe Lallement, Benjamin Iñiguez, Matthias Bucher and Ashkhen Yesayan for their involvement in this research. Finally, we would like to thank warmly Dr. Adil Koukab, Dr. Anurag Mangla, and Nikolaos Makris for the very constructive scientific discussions.

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Farzan Jazaeri and Jean-Michel Sallese

Abbreviations

Abbreviation	Expansion
AC	Alternating current
Acc	Accumulation
ADS	Advanced design system
AM	Accumulation-mode
ASIC	Application specific integrated circuit
ASD	Asymmetric double-gate
BJT	Bipolar junction transistor
BOX	Buried oxide
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
Dep	Depletion
DFT	Density functional theory
DG	Double-gate
DIBL	Drain-induced barrier lowering
EDL	Electrical double layer
FB	Flat-band
FET	Field-effect transistor
FinFET	Fin-based field-effect transistor
GAA	Gate-all-around
GCA	Gradual-channel approximation
GIDL	Gate-induced drain leakage
Hyb	Hybrid
IC	Integrated circuits
IGFET	Insulated-gate semiconductor field-effect transistor
IGN	Induced-gate noise
IM	Inversion-mode
ISFET	Ion-sensitive field-effect transistor
ITRS	International technology roadmap for semiconductors
JFET	Junction FET
JL	Junctionless
LHS	Left-hand side
MOSFET	Metal-oxide semiconductor field-effect transistor
NEGF	Non-equilibrium green's function
NW FET	Nanowire field-effect transistor

Abbreviation	Expansion
PSD	Power spectral density
QCE	Quantum confinement effect
QEB	Quantum energy balance
QHO	Quantum harmonic oscillator
QME	Quantum mechanical effect
QW	Quantum well
RHS	Right-hand side
RF	Radio frequency
RSCE	Reverse short-channel effect
SC	Semiconductor channel
SCE	Short-channel effect
SOI	Silicon-on-insulator
SS	subthreshold swing
SW	Switch
TCAD	Technology computer-aided design
VeSFET	Vertical slit semiconductor field-effect transistor
VeSTIC	Integrated circuit vesfet-based

Symbols

Symbol	Description	Unit
q	**Electron charge**	*Coulomb*
T	**Absolute temperature**	Kelvin
h	**Planck's constant**	$J.s$
$\bar{h} = h/(2\pi)$	**Reduced Planck's constant**	$J.s$
k_B	**Boltzmann's constant**	J/K
ε_0	**Permittivity of free space**	F/m
ε_{si}	**Permittivity of silicon**	F/m
ε_{ox}	**Permittivity of SiO_2**	F/m
m_e^*	**Electron effective mass**	Kg
m_h^*	**Hole effective mass**	Kg
N_c	**Effective density of states in conduction band**	m^{-3}
N_v	**Effective density of states in valence band**	m^{-3}
$g_c(E)$	**Density of states in conduction band**	$m^{-3}J^{-1}$
$g_v(E)$	**Density of states in valence band**	$m^{-3}J^{-1}$
n_i	**Intrinsic carrier concentration**	m^{-3}
E_g	**Silicon band-gap**	eV
E_i	**Intrinsic Fermi energy**	eV
E_f	**Fermi energy**	eV
E_c	**Bottom of conduction band energy level**	eV
E_{cM}	**Top of conduction band energy level**	eV
E_{vm}	**Bottom of valence band energy level**	eV
E_v	**Top of valence band energy level**	eV
σ_n	**Cross section of electrons**	m^2
σ_p	**Cross section of holes**	m^2
e_n	**Electron emission coefficient**	s^{-1}
e_p	**Hole emission coefficient**	s^{-1}
v_n	**Electron average velocity**	ms^{-1}
v_p	**Hole average velocity**	ms^{-1}
τ_c	**Average scattering time**	s
σ	**Average conductivity**	$\Omega^{-1}m^{-1}$
$J_{n,drift} = qn\mu_n$	**Drift electron current density**	Acm^{-2}
$J_{p,drift} = qp\mu_p$	**Drift hole current density**	Acm^{-2}
$J_{n,diffusion}$	**Diffusion electron current density**	Acm^{-2}
$J_{p,diffusion}$	**Diffusion hole current density**	Acm^{-2}
J_{drift}	**Total drift current density**	Acm^{-2}
$J_{diffusion}$	**Total diffusion current density**	Acm^{-2}

Symbol	Description	Unit
$f(E)$	**Fermi–Dirac statistic**	–
$D_n = \mu_n k_B T$	**Electron diffusion constant (Einstein relation)**	$m^2 s^{-1}$
$D_p = \mu_p k_B T$	**Hole diffusion constant (Einstein relation)**	$m^2 s^{-1}$
W_m	**Metal work function**	V
W_s	**Semiconductor work function**	V
χ	**Electron affinity**	V
$W_{ms} = W_m - W_s$	**Metal-semiconductor work function difference**	V
$\Delta\phi_{ms}$	**Difference between metal work function and an intrinsic semiconductor reference** $\Delta\phi_{ms} = W_{ms} - (E_f - E_i)/q = W_{ms} - U_T \ln(N_D/n_i)$	V
μ	**Free-carrier mobility**	$cm^2/V.s$
μ_n	**Free electron mobility**	$cm^2/V.s$
μ_p	**Free hole mobility**	$cm^2/V.s$
μ_0	**Low-field surface mobility**	$cm^2/V.s$
μ_{eff}	**Effective carrier mobility**	$cm^2/V.s$
U_T	**Thermodynamic voltage**	V
t_{ox}	**Oxide thickness**	m
X_{dep}	**Depletion width**	m
$C_{ox} = \varepsilon_{ox}/t_{ox}$	**Gate oxide capacitance**	F/m^2
$C_{dep} = \varepsilon_{si}/X_{dep}$	**Depletion capacitance**	F/m^2
C_{eq}	**Series combination of C_{ox} and C_{dep}**	F/m^2
N_D	**Uniform donor concentration in channel**	cm^{-3}
N_A	**Uniform acceptor concentration in substrate**	cm^{-3}
N_s	**Trap density of states**	cm^{-2}
n	**Electron density**	cm^{-3}
p	**Hole density**	cm^{-3}
T_{sc}	**Silicon thickness**	m
$T_{sc,min}$	**Minimum silicon thickness in VeSFET**	m
$T_{sc,max}$	**Maximum silicon thickness in VeSFET**	m
$C_{si} = \varepsilon_{si}/T_{sc}$	**Channel capacitance**	F
W	**Channel width**	m
h	**Channel height**	m
Q_{fix}	**Fixed-charge density**	C/m^2
Q_m	**Mobile charge density**	C/m^2
$Q_{m,s}$	**Local mobile charge density at source**	C/m^2
$Q_{m,d}$	**Local mobile charge density at drain**	C/m^2
$Q_{m,FB}$	**Local mobile charge density at flat band**	C/m^2
$Q_{m1,2}$	**Internal mobile charge densities**	C/m^2
$\overline{Q}_{m,s}$	**Global source charge density**	C/m^2
$\overline{Q}_{m,d}$	**Global drain charge density**	C/m^2
$Q_G = \overline{Q}_{m,s} + \overline{Q}_{m,d}$	**Total gate charge density**	C/m^2
$Q_{sc} = Q_m + Q_{fix}$	**Total charge density in semiconductor**	$C/m2$
Q_{ss}	**Interface charged trap density**	$C/m2$
$V_{GS,FB}$	**Flat-band gate voltage at source**	V
$V_{ch}(y)$	**Channel potential**	V
x	**Coordinate across the gates**	m
y	**Coordinate along the channel**	m

Symbol	Description	Unit
V_{GS}	**Gate to source voltage**	V
V_{DS}	**Drain-to-source voltage**	V
V_{th}	**Threshold voltage**	V
$\Psi(x)$	**Potential distribution**	V
$\Psi_s{=}\Psi(x{=}\pm\frac{T_{sc}}{2})$	**Surface potential**	V
$\Psi_0{=}\Psi(x=0)$	**Center potential**	V
E_s	**Electric field at surface**	V/m
I_{DS}	**Drain current**	A
V_{th}	**Threshold voltage**	V
V_T	**Charge threshold voltage**	V
R	**Radius**	m
θ	**Mobility reduction coefficient**	$1/V$
$\Psi_{0,FB}$	**Center potential at flat-band**	V
$\Psi_{s,FB}$	**Surface potential at flat-band**	V
Ψ_{BCP}	**Body center potential**	V
$\Psi_{BCP,min}$	**Minimum body center potential**	V
$\Psi_{s,min}$	**Minimum surface potential**	V
Ψ_{0c}	**Critical value for the center potential**	V
Ψ_{sc}	**Critical value for the surface potential**	V
Ψ_{ox}	**Oxide potential**	V
Ψ_{ext}	**Extremum potential across two gates**	V
X_{ext}	**Extremum position across two gates**	m
E	**Electric field**	V/m
E_s	**Surface electric field**	V/m
E_0	**Center electric field**	V/m
E_{ox}	**Electric field in the oxide**	V/m
E_x	**Longitudinal electric field**	V/m
E_y	**Lateral electric field**	V/m
E_t	**Trap-energy level**	eV
$V_{GS,crit}$	**Critical value for the gate potential**	V
$I_{critical}$	**Critical value for the drain-to-source current**	A
g_{ds}	**Drain trans conductance**	Ω^{-1}
g_m	**Gate transconductance**	Ω^{-1}
V_{bi}	**Built-in potential**	V
g_{ch}	**Local channel conductance**	Ω^{-1}
$S_{\Delta I_{DS}}$	**PSD of drain current thermal noise**	A^2/Hz
$S_{\Delta I_G}$	**PSD of induced gate noise**	A^2/Hz
$S_{\Delta I_{DS}\Delta I_{G^*}}$	**PSD of cross-correlation noise**	A^2/Hz
$C_{GD}{=}\partial Q_G/\partial V_{DS}$	**Gate–drain intrinsic capacitance**	F/m^2
$C_{GG}{=}\,\partial Q_G/\partial V_{GS}$	**Intrinsic gate capacitance**	F/m^2
$C_{DD}{=}\partial\overline{Q}_{m,d}/\partial V_{DS}$	**Drain–drain capacitance**	F/m^2
$C_{SD}{=}\partial\overline{Q}_{m,s}/\partial V_{DS}$	**Source–drain capacitance**	F
$C_{DG}{=}\partial\overline{Q}_{m,d}/\partial V_{GS}$	**Drain–gate capacitance**	F/m^2
$C_{SG}{=}\partial\overline{Q}_{m,s}/\partial V_{GS}$	**Source–gate capacitance**	F
ω	**Angular frequency**	rad/s
f	**Frequency**	Hz