1 Introduction

1.1 The Birth of the Transistor

Since its invention in 1907 by Lee de Forest, the vacuum tube has been a major driver for electronics and communications technologies. However, vacuum tubes have conceptual limits. Besides being quite expensive, they have reliability issues, high energy consumption, and miniaturization limits. To address these limitations, AT&T, one of the main US phone companies, tasked its R&D unit – Bell Laboratories – with the development of an innovative device that would be cheaper, smaller, and more reliable – in short, a good substitute for the vacuum tube.

The initial idea for "transistors" came from Edgar Julius Lilienfeld in 1925 [6]. The scientist patented in Canada (1925) and successively in the United States (1928) the first field-effect semiconductor device designed to change the resistivity with applied voltages. However, due to the lack of dedicated technology, Lilienfeld never had the chance to validate his concept. It's interesting to note that his transistor idea was quite similar to today's accumulation-mode (AM) transistors.

The point-contact transistor built by John Bardeen and Walter Brattain at Bell Laboratories in the United States in December 1947 was the first solid-state transistor ever created. The two scientists, led by the physicist William Bradford Shockley, discovered the new amplification device while working on theory and experiments on solid-state materials (germanium in this case). This first proof of "controlled resistance" and "amplification" in a solid-state device is considered as the birth of the transistor, and its inventors were jointly awarded the Nobel Prize in physics in 1956 for this achievement.

After invention of the point-contact transistor, Bell Labs followed up with design and fabrication of solid-state amplifiers, gaining a deep understanding of transistors physics. A fully working junction transistor based on Shockley's design, consisting of adjacent semiconductors junctions, was fabricated in 1951 [7]. In 1954, at Texas Instruments Gordon Teal demonstrated the first silicon transistor using the knowledge gained by growing high purity crystals while working at Bell Labs.

1.2 The Metal-Oxide–Semiconductor Field-Effect Transistor

By the end of 1950s, all solid-state transistors were bipolar junction transistors (BJT). However, in 1959, John Atalla and Dawon Kahng at Bell Labs operated the

field-effect transistor anticipated by Lilienfield and Shockley, called the insulated-gate semiconductor field-effect transistor (IGFET). The first version of IGFET was the metal-oxide–semiconductor field-effect transistor (MOSFET) and has been used since, although the metal was replaced for many years by doped polycrystalline silicon (poly-Si) – from where the name metal insulator semiconductor field-effect transistor (MISFET). The idea is to modulate the conductivity of the channel (between source and drain) via voltage on the gate electrode. The conductivity in such MISFETs can be modulated in three different ways. One is by depleting the doped semiconductor from its majority carriers, which targets the well known junction FET (JFET). Another option is to enhance the majority carrier concentration, which is known as the accumulation-mode MOSFET. Last, the most popular way conductivity can be modulated is by using inversion-mode (IM) MOSFETs, where the gate voltage is used to invert the semiconductor in a region very close to the semiconductor–insulator interface. Among the technologies developed over time, CMOS technology has proven to be one of the most important achievements in engineering history.

1.3 Moore's Law, Limits of CMOS Scaling, and Alternative MOSFET Structures

1.3.1 Scaling in Bulk MOSFETs

With device scaling in MOSFETs, performance improvements in large-scale integrated circuits (LSI) have been impressive. In particular, reducing the device dimensions has greatly improved the performance of integrated circuits. For the past three decades, scaling of CMOS devices has been the key factor for improving device density, speed, and power reduction in integrated circuits. Scaling of CMOS technology is the main driving force in the semiconductor industry. However, scaling of conventional bulk MOSFETs is also reaching some intrinsic limits.

Scaling improves cost, speed, and power per function with every new technology generation. Gordon Moore made an empirical observation in the 1960s that the number of devices on a chip will double every 18 months [5]. The gate length of a MOSFET has been reduced from around $10\,\mu m$ in 1970 to $14\,nm$ in today's technology node. Maintaining the pace of downscaling is the driving force for further development of the semiconductor industry. However, improvement in performance through miniaturization must cope with severe short-channel effects [8, 9] and inherent limitations of silicon [10]. Decreasing the minimum feature size of the MOSFET brings forward some critical issues, which, in addition to the technology, are related to the device principle. For instance, higher gate capacitance is needed to drive more current while the supply voltage is decreasing. Similarly, to avoid destructive breakdown and leakage current in SiO_2 films thinner than $1.5\,nm$, high-k

dielectrics i.e., HfO_2 are used in place of SiO_2 [11–13]. The most critical issues that come along with miniaturization are as follows:

- Subthreshold swing degradation
- Drain-induced barrier lowering (DIBL)
- Random dopant fluctuations (RDF)
- Threshold voltage roll-off
- Hot carriers
- Reliability issues
- Gate leakage current.

The traditional approach to addressing these drawbacks is to increase the doping density in the channel and the gate capacitance. However, some semiconductor foundries have started investigating various solutions while proposing new device structures such as the fully depleted SOI MOSFET [14], the double-gate (DG) MOSFET [15], SiGe MOSFET [16], junctionless nanowire FETs [1], vertical slit FET [17–19], tunnel FETs [20], and even quantum dot devices [21].

As the density is further increased, extrinsic elements are becoming extremely important as well. These require innovative integration schemes such as vertical transistors and monolithic 3D integration [17, 18]. In the same spirit, a generic device concept known as the vertical slit field-effect transistor (VeSFET) was proposed by Wojciech Maly [17]. This 3D architecture aimed at being integrated in SOI technology was conceptualized in different configurations such as bipolar transistors and IM FETs for instance [22, 23].

1.3.2 Silicon-on-Insulator MOSFETs

Silicon-on-insulator (SOI) MOSFETs were the first category of new transistor architecture to disrupt the classical bulk CMOS evolution. In the 2000s, some companies (e.g., IBM, AMD) started using SOI substrates. Fully depleted SOI MOSFETs scale in a very similar way as bulk devices, but the SOI MOSFET has several advantages compared to its bulky counterpart, especially for short-channel effects. The buried oxide cuts most of the bulk leakage current that dominates in downscaled bulk MOSFETs due to the relatively large DIBL and subthreshold swing (SS), and the smaller source and drain junction areas minimize the junction capacitances, which helps increase the frequency and decrease the dynamic power consumption [24].

Another advantage of SOI technology is the use of multigate transistors with different topologies: double-gate, trigate, Ω-gate, π-gate, and gate-all-around (GAA), and so on. These devices have superior performance due to excellent control of short-channel effects giving rise to steeper subthreshold slope and lower DIBL [15].

The first commercially available CMOS technology making use of multigate architecture, the so-called trigate transistors, was introduced in 2012 by Intel for the 22 *nm* node. The trend was followed successively by TSMC in late 2013. Samsung

and Global Foundries announced their FinFET technology for the 12 *nm* node in September 2017. In conclusion, fully depleted SOI technology is expected to be the short-term CMOS-compatible solution that combines low-power consumption and high CMOS circuit performance.

1.4 The Junctionless Concept

Although these devices based on ultrathin channels have been proposed and developed, the fabrication complexity and the related increased manufacturing costs explain why most of them are still far from being used in large-scale production.

The *pn* junction is a key element in MOSFET technology as it is used to isolate the device from the substrate and restrict the current flow in the inversion layer. Formation of source/channel and drain/channel junctions with high doping concentration gradients has been a critical issue in designing short-channel devices. In addition, controlling the source/drain junction depths at the nanometer scale is very difficult. For example, in a current CMOS technology, the doping must switch from a *n*-type doping higher than $1 \times 10^{19}\ cm^{-3}$ in the source/drain extensions, to a *p*-type doping of about $1 \times 10^{18}\ cm^{-3}$ in the channel, within a few nanometers [1]. An ultrafast annealing process and low thermal budged are needed to meet these requirements. From this point of view, having a device without a junction can be technologically and economically beneficial. Getting rid of this technological step was the main motivation for the integration of Schottky contacts for source and drain [25, 26].

Among these arrangements, one configuration of interest in this text is the so called junctionless field-effect transistor (JLFET). This type of device consists of a uniformly doped channel from source to drain [1, 27] i.e., they do not have a *pn* junction for source and drain, which helps get rid of abrupt doping profile issues.

The first experimental evidence came from Jean-Pierre Colinge and coworkers in 2010 [1] (see Figure 1.1) who proposed a planar triple-gate architecture implemented in ultrathin body SOI in 2009 [28]. It is worth noting that the principle of operation of junctionless FETs devices is similar to that of the JFETs invented by Shockley in 1952, in that they are voltage-controlled resistors based on majority carriers and without source and drain junctions. However, in JFET, some junctions are implemented for the gates reversed biased to control the channel (modeling of JFET will be revisited in Chapter 12).

1.4.1 Working Principle of Junctionless MOSFETs

The electrical characteristics of the junctionless transistor look very similar to the regular MOSFET i.e., for an *n*-type channel device the current increases when increasing the gate-to-source voltage. However, the principle of operation of junctionless double-gate MOSFETs is based on a current flowing in the volume of a heavily doped silicon layer and not at the $Si–SiO_2$ interface as in regular MOSFETs. In addition, the charge-voltage relationship is fundamentally different. Indeed, an

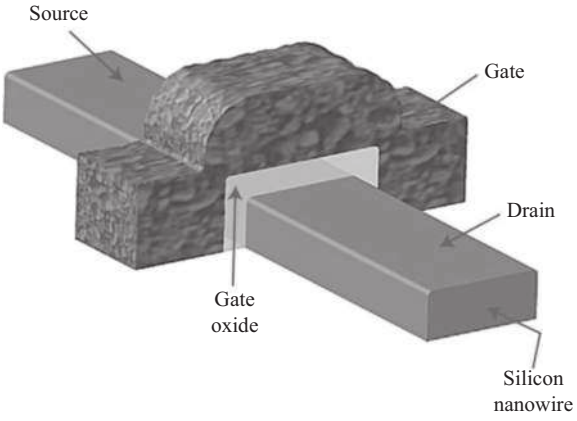

Figure 1.1 A junctionless double-gate MOSFET concept presented by Colinge et al. [1]. Reprinted from [1] with permission.

additional quadratic term comes into play in the junctionless double-gate MOSFET when operating below the flat-band.

The junctionless FET is made of a heavily doped semiconductor layer isolated from the gate electrodes by a thin dielectric, as for the IM MOSFET. However, besides this common feature, many differences exist between these two devices. The electrical conductivity in junctionless FETs is governed by majority carriers in the volume rather than by an inversion layer as in junction-based MOSFETs. Therefore, the channel conductance is modulated by depleting or enhancing majority carriers in the semiconductor layer. Whereas in inversion-mode MOSFETs, the flat-band voltage means that the device is turned off, in junctionless FETs flat-band means that the channel is neutral and therefore very conductive (the free-carrier density is almost equal to the doping density; see Figure 1.2). In fact, for *n*-type channels, the flat-band condition is situated above the threshold voltage ($V_{th} < V_{GS,FB}$). When the gate potential is below the threshold voltage in an *n*-type channel, the channel is depleted from majority carriers. As the gate voltage is further decreased, full depletion can be achieved and the device is turned off (see Figure 1.2a). On the other hand, when the gate potential is above the threshold voltage but still below the flat-band voltage, the channel region is partially depleted (see Figure 1.2c). Finally, increasing the gate voltage above the flat-band creates an accumulation channel that also "behaves" more or less as the inversion channel of an inversion-mode MOSFET.

Work function engineering is obviously critical in junctionless FETs since for the unbiased device to be in an *off*-state, the work function difference between the gate material and the doped semiconductor must be tuned so the channel is fully depleted at $V_{GS} = 0$ (see Figure 1.2a).

Figure 1.3a shows the drain current versus the gate voltage in *n*- and *p*-type devices having a width of 30 *nm* and a length of 1 μm. Figure 3b and c shows the experimental output characteristics of *n*- and *p*-channel gated resistors, respectively.

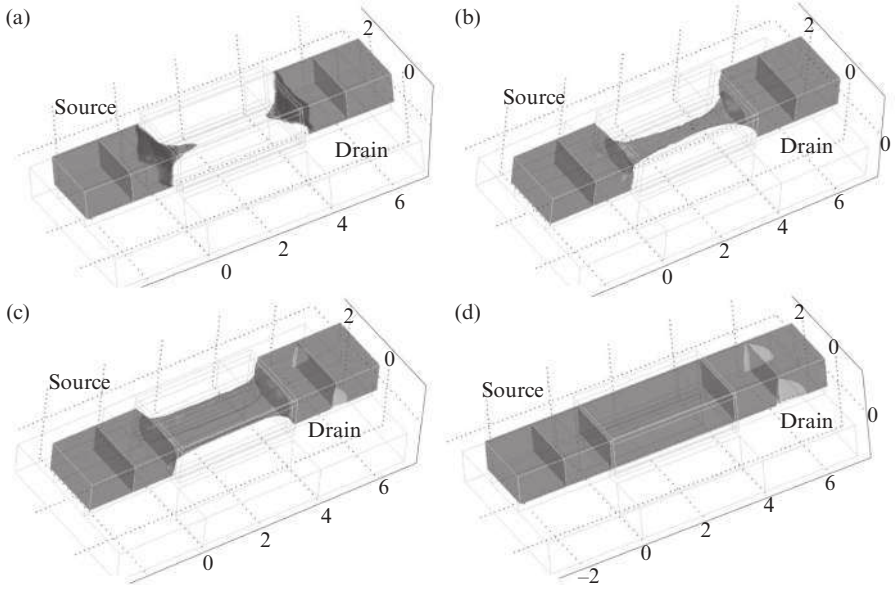

Figure 1.2 Electron concentration contour plots in an *n*-type junctionless gated resistor (a)–(d). Plots result from simulations carried out for a drain voltage of 50 mV and for different gate-voltage values: (a) below threshold, the channel region is depleted of electrons; (b) at threshold, a string-shaped channel of neutral *n*-type silicon connects source and drain; (c) above threshold, the channel neutral *n*-type silicon expands in width and thickness; (d) when a flat energy band situation is reached, the channel region has become a simple resistor. The plots were generated by solving the Poisson, drift-diffusion, and continuity equations. The device has a channel width, height, and length of 20, 10, and 40 nm, respectively. The *n*-type doping concentration is 10^{19} cm^{-3}. Reprinted from [1] with permission.

1.4.2 Diversity in Junctionless Architectures

The gate geometries of semiconductor field-effect devices have been improved to enhance their performance. Thus, junctionless architectures can have different shapes such as circular nanowires, multiple-gate nanowires [28], or vertical slit transistors (VeSFETs) [19]. The first working junctionless transistor was implemented as trigate silicon nanowire on SOI substrate [29].

Junctionless Double-Gate MOSFETs

Among the junctionless architectures that can sustain scalability is the double-gate topology (JL DG MOSFET). Despite its "simple" design, this is one of the most difficult architectures to implement because it requires precise alignment of the independent gates. Nevertheless, from a modeling point of view, the main advantage is to treat the device as a simple 1D system.

Junctionless Nanowire FETs

One-dimensional nanostructures such as nanowires and nanotubes are very attractive building blocks for nanoelectronics because of their relatively simple fabrication

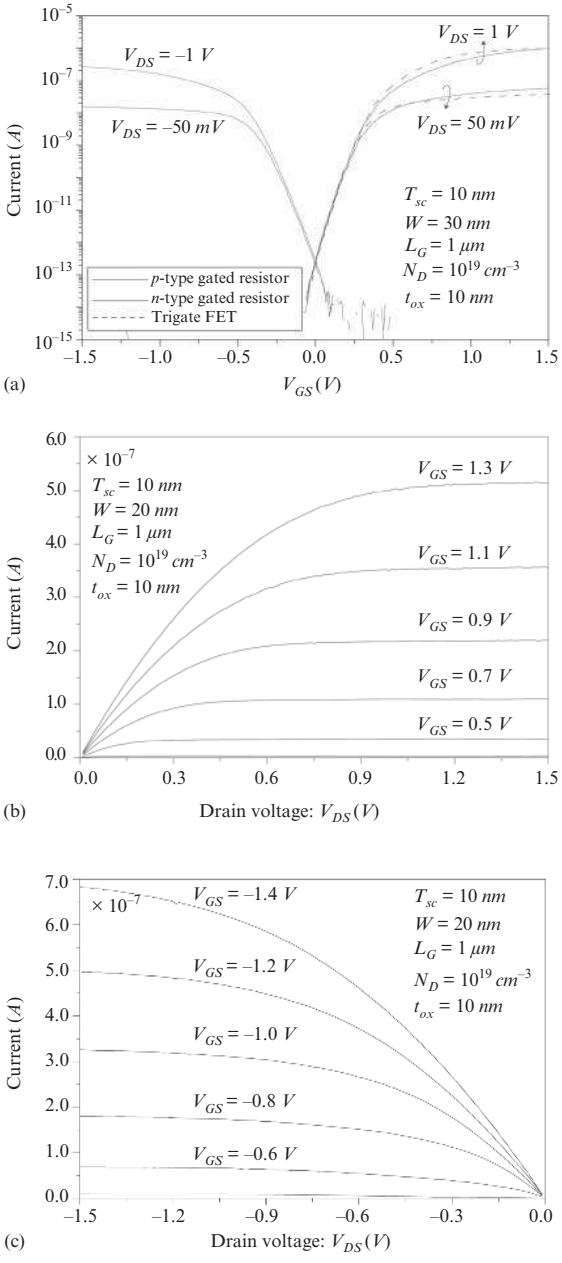

Figure 1.3 Current–voltage characteristics: Drain current versus gate voltage for drain voltages of +50 *mV* and +1 *V*. The width of the device is 30 *nm*. (a) The curve for a classical trigate FET is shown for comparison. Measured output characteristics of gated resistors: drain current versus drain voltage for different values of gate voltage for (b) an *n*-channel gated resistor and (c) a *p*-channel gated resistor. The width of the nanowires, *W*, is 20 *nm* and the gate length, L_G, is 1 μm. Reprinted from [1] with permission.

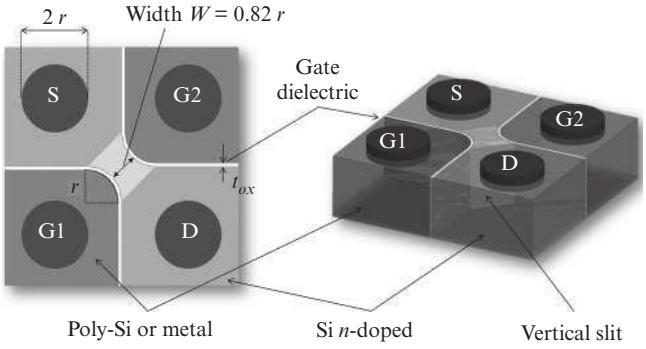

Figure 1.4 The architecture of a single-cell *n*-type VeSFET, as proposed by Maly [17], for high-density integration. Reprinted from [17] with permission.

processes combined with excellent electrostatic control of the channel. Indeed, junctionless nanowires can be obtained from different techniques (some of them relying on self-limited oxidation of silicon), which is obviously an advantage in academia for instance. Although electrical characteristics of double-gate (DG) and nanowire (NW) junctionless FETs (JL FETs) are quite similar, the way analytical models are derived is quite different and becomes more complex for nanowires due to analytical formulation of the Poisson–Boltzmann equation in cylindrical coordinates.

Junctionless Bulk FinFETs

Likewise Inversion mode bulk FinFETs which have been fabricated and used in real circuits (Intel), junctionless bulk FinFETs could be effectively implemented in bulk CMOS technology, getting rid of SOI technology constraints. Analysis by Han and coworkers [30, 31] suggested that short-channel junctionless FinFET transistors integrated in bulk silicon can perform as inversion-mode FinFETs and outperform SOI-based junctionless FinFETs, especially in regards to the off-current, DIBL, and subthreshold swing (SS). This means a cheaper bulk technology could be used to integrate junctionless FETs.

Junctionless Vertical Slit FETs

In addition to nanowire and double-gate shapes, the concept of junctionless FET was introduced by Wojciech Maly [17] in the name of VeSFETs. This new type of transistor is expected to relax lithography constraints by using highly regular arrays to achieve 3D integration at the nanometer scale (see Figure 1.4). All the devices in a VeSTIC can be arranged in regular arrays, evenly spaced, forming a "transistor canvas" (see Figure 1.5), with lower manufacturing costs and faster design capabilities [32]. Moreover, digital [33, 34] and analog [35] functions are expected to be easily integrated with a regular layout. Potentially, every transistor could be interconnected by upper and bottom terminals. In addition to the junctionless architecture, the "vertical slit" topology could also be applied to inversion-mode FETs and bipolar devices.

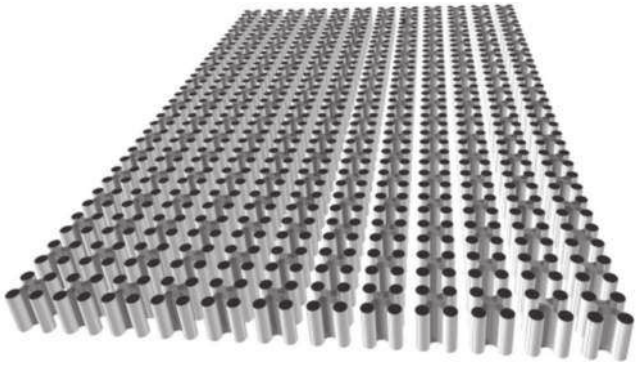

Figure 1.5 VeSFET in canvas allowing contacts both above and below the active device layer. Reprinted from [19] with permission.

Today, the principle operation has been proven [19] together with well controlled short-channel effect. It has been demonstrated [32, 33] that single independent gate VeSFETs can also act as AND and OR gates by tuning the slit width, providing a 60 percent area saving for a NAND logic gate.

1.5 Short-Channel Effects in Junctionless FETs

In addition to mitigating source and drain junctions implementation constraints, the principle of operation of junctionless FETs is expected to alleviate the short-channel drawbacks of MOSFETs. For instance, in the *off*-state, the charge depletion induced by the gate extends to the end of the gate electrode, inducing a longer resistive channel and lowering the *off*-state current. Conversely, in the *on*-state, the homojunction between the source/drain and the channel is expected to lower the access resistance. In addition, inversion-mode MOSFETs are sensitive to the semiconductor/gate insulator interface whereas for junctionless transistors the current flows in the "center" of the channel, meaning surface and roughness scattering should be less of a concern.

It has been reported that thin-film double-gate devices in AM have better short-channel effects and related DIBL than inverted channel multigate FETs [36], meaning that junctionless devices could also be more immune to short-channel effects.

The DIBL is another critical parameter that affects both static and dynamic operation in the off-state. Numerical simulations [37–41] and analytical solutions for DIBL in junction-based double-gate MOSFETs [42–48] have been done, some of them making use of the conformal mapping technique [48, 49]. A comparison of DIBL and subthreshold swing versus physical gate length for junctionless and IM multigate FETs is shown in Figure 1.6 [28]. As can be seen, the junctionless multigate FET has better short-channel characteristics than the inversion-mode device.

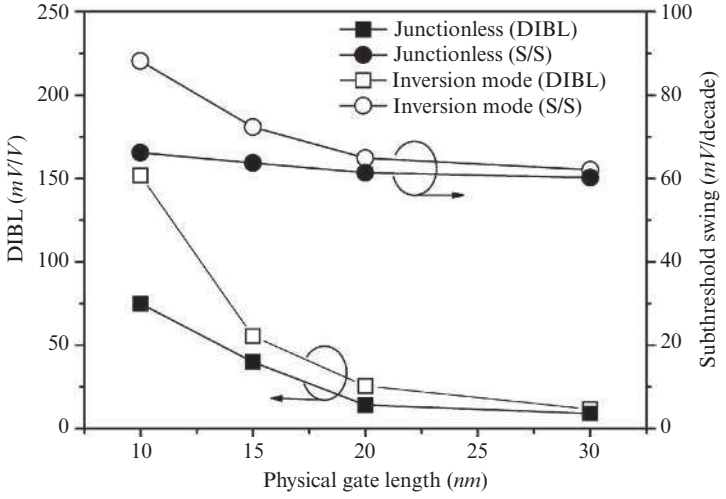

Figure 1.6 DIBL and subthreshold swing at $V_{DS} = 50\,mV$ in junctionless and regular IM devices with $T_{si} = 5\,nm$. Reprinted from [28] with permission.

However, there are still some technological limitations that have to be quantitatively assessed in order to optimize the device performance while scaling down its dimensions. Increasing the doping to obtain a high *on*-current at flat-band must be mitigated in regard to other constraints. Indeed, one should be able to set the channel in full depletion to turn it off, which might be impossible if the channel thickness and/or the doping density are too high [50, 51]. In addition, the constraint on doping could also be a major hindrance to improve figures of merit such as time delay and power consumption, as discussed in [52].

1.6 Mobility in Junctionless FETs

The free-carrier mobility in junctionless devices was reported to be higher than in bulk semiconductor [53], still increasing with the gate bias above flat-band, in contrast to what is expected in highly doped semiconductors subjected to enhanced Coulomb scattering from ionized dopants. Upon measurement, a 40 to 110 percent increase in mobility compared to the values in bulk silicon for doping levels ranging from $1 \times 10^{19}\,cm^{-3}$ to $4 \times 10^{19}\,cm^{-3}$ has been reported. This unexpected higher mobility was attributed to lower Coulomb scattering due to a screening of ionized donors. Sore et al. [54] reported that mobility is also dependent on the channel width and that the surface roughness could be the dominant scattering mechanism, in addition to ionized impurities.

However, comparison of long-channel trigate inversion-mode FETs and junctionless FETs in [55] revealed a lower current in junctionless FETs, as for g_m and g_{ds}, which was attributed to lower mobility.