Electromigration in Metals

Learn to assess electromigration reliability and design more resilient chips in this comprehensive and practical resource. Beginning with fundamental physics and building to advanced methodologies, this book enables the reader to develop highly reliable on-chip wiring stacks and power grids. Through a detailed review on the role of microstructure, interfaces, and processing in electromigration reliability, as well as characterization, testing, and analysis, the book follows the development of on-chip interconnects from microscale to nanoscale. Practical modeling methodologies for statistical analysis, from simple 1D approximation to complex 3D description, can be used for step-by-step development of reliable on-chip wiring stacks and industrial-grade power/ground grids. This is an ideal resource for materials scientists and reliability and chip design engineers.

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Frontmatter
More Information

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Fundamentals to Nano-Interconnects

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To Hillard B. Huntington
for his pioneering studies of electromigration

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Frontmatter
More Information

Contents

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Paul S. Ho , Chao-Kun Hu , Martin Gall , Valeriy Sukharev
Frontmatter
More Information

Colour plates section to be found between pp. 210 and 211

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Preface

The study of electromigration (EM) can be traced to the mid-1900s with experiments to observe the effect of electrical current on mass transport in solid and liquid metals. This was followed by theoretical studies to analyze the "electron wind" driving force and its effect on diffusion due to the scattering of the electrons or, more generally, the charge carriers with the mobile ions. The subject took a drastic turn in the 1960s when EM was found to induce crack formation, leading to failure of aluminum conductor lines in silicon chips. This was a serious reliability problem for the microelectronics industry, coming at a time when the industry was at the beginning to develop very-large-scale integration (VLSI) of integrated circuits. This has generated great interests to study EM in thin films and metal lines, which has distinct characteristics. For metal lines on a chip, the current density can be much higher (100× or more) than in bulk metals due to substrate cooling, but diffusion occurs at a lower temperature, about 0.5 of the absolute melting point T_m, where it is dominated by structural defects, such as surfaces, interfaces, and grain boundaries. In addition, the confinement of the interlevel dielectrics and the silicon substrate can sustain mechanical stresses to counteract EM to reduce mass transport and damage formation.

As semiconductor technology continued to develop, Cu damascene structures were introduced to replace Al interconnects in 1997, and subsequently low permittivity (or "low k") materials were implemented as interlevel dielectrics. This changed the basic material, structure, and process of on-chip interconnects, with EM lifetimes being predicted to degrade by half for every technology node, even with a constant current density. With device scaling, the dimensions of the Cu lines continue to reduce to the nanoscale, significantly affecting the Cu microstructure and adding complexity and the demand for EM reliability. Responding to the technological needs, EM studies of Cu interconnects were greatly extended to provide better understanding and to develop effective approaches such as interfacial engineering and alternate metallization for improving the EM reliability at the nanoscale.

The study of EM includes a wide range of topics, from materials science and semiconductor device physics to statistics and probability, making it a truly multidisciplinary subject. The physics of failure and the stochastic process are topics of active research by experts in different areas of science and engineering. The aim of this book is to provide a comprehensive resource for those interested in the fundamentals of EM as a physical phenomenon and in its role as a major problem in chip reliability. We hope that this book will be useful for materials scientists, reliability

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Frontmatter
More Information

engineers, and chip physical design professionals, as well as for the increasing number of graduate students pursuing interdisciplinary research of materials science and electrical engineering.

This book is organized into nine chapters extending from the basic studies in bulk metals to on-chip interconnects from the microscale to the nanoscale. The group of the first four chapters reviews the basic studies, starting from an introduction to EM in Chapter 1, followed by a review of the theory and the studies of bulk metals in Chapter 2, including a kinetic analysis of the solute effect. In Chapter 3, the discussion is focused on the analysis and X-ray diffraction measurements of thermal stresses induced by the dielectric and substrate confinement in Al and Cu lines, and on showing how substantial hydrostatic stresses can be induced, leading to void formation. This is followed by Chapter 4, analyzing the kinetics of mass transport under EM and thermal stresses, leading to Korhonen’s equation and the Blech “short length” effect. Here, analytical solutions and simulations are presented in one dimension (1D) to analyze the microstructure and stress effects on damage formation and early failures under EM.

The second part of this book contains five chapters focusing on advanced topics relating to the scaling effects on EM at the nanoscale, including microstructure evolution, massive-scale statistical tests, and power grid applications. Starting from Chapter 5, the EM characteristics and reliability studies of Cu conductor lines are reviewed and assessed as scaling continues to the nanoscale. Several innovative approaches have been developed to improve EM reliability for Cu interconnects, including the use of cap layers and alloying effects. In Chapter 6, we investigate the scaling effect on microstructure evolution using a high-resolution electron diffraction technique to examine Cu interconnects to 22 nm linewidth and Co interconnects to 26 nm linewidth. Based on the observed microstructures, a Monte Carlo simulation was developed based on total energy minimization to project the scaling effect on grain growth and the implication on EM reliability for future technology nodes. In Chapter 7, the analysis of EM and stress evolution is generalized from 1D to 3D damascene interconnects, where a physics-based simulation is set up to analyze the microstructure effects on stress evolution and void formation. Results from the simulation are combined with scanning and transmission electron microscopy (SEM/TEM) experiments to study void nucleation, migration, growth, and shape evolution leading to interconnect degradation.

With continued scaling to the nanoscale, the statistical nature of damage formation becomes important to assess EM reliability, which is dominated by the early failures of the weakest links. This topic is discussed in Chapter 8, presenting a novel approach based on the Wheatstone Bridge technique to perform statistical EM tests on a massive scale to detect early failures. In Chapter 9, we conclude with a discussion of a novel approach to assess EM reliability for power grid systems based on a mesh model to account for system redundancy and to track EM degradation in multibranch interconnect trees across the die. Such problems are important for future development of reliable Cu interconnects as scaling continues to expand the wiring structure to the material limit at the nanoscale.

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Over the years, all of us have been fortunate to work and interact with many colleagues who helped to broaden and improve our understanding of the fundamentals of EM and its role in interconnect degradation, notably Robert Rosenberg, Matt A. Korhonen, Tony Oates, King-Ning Tu, and William D. Nix. We acknowledge the fruitful collaborations with many brilliant scientists and engineers; in particular, Hisao Kawasaki, Ehrenfried Zschech, Ennis Ogawa, Steve Anderson, Carl V. Thompson, Farid N. Najm, Armen Kteyan, and Junjun Liu have provided discussions and ideas to generate many interesting and important experimental and theoretical results described in this book. We thank the members of the University of Texas at Austin group, particularly Steve S. T. Hu, D. W. Gan, S. H. Rhee, L. J. Cao, M. Hauschildt, J. Kasthurirangan, and I. S. Yeoh, who have contributed to the research results cited in this book. The research support from the National Science Foundation, the Semiconductor Research Corporation, SEMATECH, IBM, Motorola, Intel, Siemens EDA (formerly the Mentor Graphics Corporation), and the University of Texas at Austin is gratefully acknowledged. Part of the work for Chapter 5 was performed by Research Alliance Teams at various IBM Research and Development Facilities, which is gratefully acknowledged. We thank especially Sarah Strange and Julia Ford of the Cambridge University Press for their continuous help with the book preparation. Finally, and most importantly, we thank our wives for their patience and understanding while we worked to complete this book.