Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs

Understand the theory, design, and applications of the two principal candidates for the next mainstream semiconductor-industry device with this concise and clear guide to FD/UTB transistors.

This book

- Describes FD/SOI MOSFETs and 3-D FinFETs in detail
- Covers short-channel effects, quantum-mechanical effects, and applications of UTB devices to floating-body DRAM and conventional SRAM
- Provides design criteria for nanoscale FinFET and nanoscale thin- and thick-BOX planar FD/SOI MOSFET to help reduce technology development time
- Projects potential nanoscale UTB CMOS performances
- Contains end-of-chapter exercises

For professional engineers in the CMOS IC field who need to know about optimal nonclassical device design and integration, this is a must-have resource.

Jerry G. Fossum is Distinguished Professor Emeritus of Electrical and Computer Engineering at the University of Florida, Gainesville, and a Fellow of the IEEE. He won the IEEE/EDS J. J. Ebers Award in 2004 for "outstanding contributions to the advancement of SOI CMOS devices and circuits through modeling."

Vishal P. Trivedi is a Member of the Technical Staff and a Distinguished Innovator at Freescale Semiconductor, Inc., and a Senior Member of the IEEE.

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Sorin Cristoloveanu, CNRS, Grenoble, France

"This is a timely book about SOI MOSFETs and FinFETs written by one of the leading authorities in the field and his former student. Since FinFETs have started being implemented by various companies in production, there is a need for clear understanding of the design trade-offs of such devices. Prof. Fossum, who has done seminal work on modeling SOI MOSFETs since the 1980s, provides a clear elucidation of the physics of these devices. Graduate students, faculty and industrial practitioners should benefit from the pedagogy in this book."

Sanjay Banerjee, University of Texas at Austin

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Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs

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Preface

The computer revolution (i.e., faster, smaller, and cheaper computers), and the technologies it has enabled (e.g., the Internet, laptops, smart phones), have been driven by continued size-scaling of the CMOS transistors in the constituent integrated circuits (ICs, e.g., the microprocessor) of the computer. This scaling, which has doubled the transistor density on the CMOS IC chip about every two years, has been achieved by simply ratioing the dimensions and related parameters of the basic, classical transistor structure (i.e., the planar single-gate MOSFET in bulk silicon or partially depleted SOI) (Taur and Ning, 2009) as improvements in lithography enabled reduced minimum feature size. The CMOS devices have now become so small (e.g., gate lengths are 30–40 nm) that this straightforward scaling is no longer possible, mainly because of fundamental limitations in reliable doping of the classical MOSFET. Thus, continued CMOS scaling will require a new, nonclassical transistor structure with ultra-thin body (UTB) that avoids these limitations. The first concrete evidence of the transition to a UTB transistor structure is Intel Corporation's adoption of the "trigate transistor" (or FinFET) (Auth *et al.*, 2012) for 22 nm CMOS technology and beyond.

This book details the fundamental physics of silicon-based UTB MOSFETs, overviews their designs, with links to the process integration, and projects potential nanoscale UTB-CMOS performance. The presentations are facilitated by the authors' process/physics-based compact model for double-gate MOSFETs, UFDG (Appendix). This book is suitable as a textbook for a one-semester graduate or senior-undergraduate university course, as well as for a fundamental guide to optimal non-classical device design and integration for professional engineers in the CMOS IC field. The prerequisites are good backgrounds in basic semiconductor device physics (e.g., as in Sze and Ng (2007)) and in fundamentals of classical bulk-Si MOSFETs (Taur and Ning, 2009). In fact, this book is intended to be a supplementary text for the latter book.

The authors acknowledge the SOI-related works of many colleagues, which provided the bases of much of this book. Special thanks are given to Professor Fossum's former Ph.D. students who so contributed: Shishir Agrawal, Duckhyun Chang, Meng-Hsueh Chiang, Jin-Young Choi, Siddharth Chouksey, Murshed Chowdhury, Lixin Ge, Keunwoo Kim, Seung-Hwan Kim, Srinath Krishnan, Hyung-Kyu Lim, Zhichao Lu, Mario Pelella, Dongwook Suh, Surya Veeraraghavan, Glenn Workman, Ji-Woon Yang, Ping Yeh, Weimin Zhang, and Zhenming Zhou; and to Leo Mathew who has provided us

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We are also grateful to our families. Professor Fossum especially thanks his wife, Mary Fossum, for unrelenting support of his "SOI obsessions." Dr. Trivedi especially thanks his parents (Pareexit and Hansa Trivedi), brother (Vaibhav), sister-in-law (Krushangi), and niece (Eesha) for their constant love, care, and support.

Physical constants

Description	Symbol	Value and unit
Electronic charge	q	$1.6 \times 10^{-19} \text{ C}$
Boltzmann's constant	k	$1.38 \times 10^{-23} \text{ J/K}$
Vacuum permittivity	ε ₀	$8.85 \times 10^{-14} \text{ F/cm}$
Silicon permittivity	$\epsilon_{\rm Si}$	1.04×10^{-12} F/cm
Oxide permittivity	ε _{ox}	3.45×10^{-13} F/cm
Si ₃ N ₄ (spacer) permittivity	ε _{sp}	$6.64 \times 10^{-13} \text{ F/cm}$
Planck's constant	h	$6.63 \times 10^{-34} \text{ J-s}$
Free-electron mass	m_0	$9.1 \times 10^{-31} \text{ kg}$
Thermal voltage $(T = 300 \text{ K})$	kT/q	0.0259 V
Silicon electron affinity	χsi	4.05 eV
Silicon bandgap	Eg(Si)	1.12 eV
Silicon intrinsic carrier concentration $(T = 300 \text{ K})$	n _i	$1.33 \times 10^{10} \text{ cm}^{-3}$
Silicon effective density of states in conduction band $(T = 300 \text{ K})$	N _c	$\sim 2.8 \times 10^{19} \text{ cm}^{-3}$
Silicon effective density of states in valence band $(T = 300 \text{ K})$	N_v	$\sim 1.0 \times 10^{19} \text{ cm}^{-3}$

Note the values (at T = 300 K) listed for n_i , N_c , and N_v . There is inconsistency in the archival literature among these constants. The given value for n_i , which is lower than commonly presumed (Taur and Ning, 2009), was taken from unpublished measurements done by C. T. Sah *et al.* in 1974 at the University of Illinois; correspondingly, $E_{g(Si)}$ was measured at 1.12 eV, which is the commonly accepted value. The given values for N_c and N_v , which are common, are indicated to be crude approximations because they are not consistent with n_i and $E_{g(Si)}$ in the parabolic band-based expression for $n_i(E_g, N_c, N_v, T)$ (Taur and Ning, 2009).

Symbols

a _f	FinFET fin aspect ratio	
β	coefficient for surface-roughness-limited mobility model	V ³ /cm ³ -s
β	term in C _{ifw} model	radian
b _i	variational parameter of jth subband	
$\dot{b_0}$	variational parameter of ground-state subband	
χsi	electron affinity	eV
C _b	body capacitance (per unit area)	F/cm ²
CB	composite body capacitance	F
C _{b(eff)}	effective body capacitance (per unit area)	F/cm ²
C _{bf}	BOX fringe capacitance (per unit width)	F/cm
C _d	depletion capacitance (per unit area)	F/cm ²
C _G	MOSFET gate capacitance (per unit area)	F/cm ²
Ci	inversion-layer capacitance (per unit area)	F/cm ²
C _{if}	inner-fringe capacitance (per unit width)	F/cm
Cof	outer-fringe capacitance (per unit width)	F/cm
Cox	gate-oxide capacitance (per unit area)	F/cm ²
Coxb	back-gate oxide capacitance (per unit area)	F/cm ²
Coxf	front-gate oxide capacitance (per unit area)	F/cm ²
C _{S/D}	source/drain-junction capacitance (per unit area)	F/cm ²
$\Delta \phi_0$	drain bias-induced increase in channel potential	V
$\Delta \phi_{0(sb)}$	drain bias-induced increase in back-surface potential	V
$\Delta \phi_{0(sf)}$	drain bias-induced increase in front-surface potential	V
$\Delta \phi_{1(\max)}$	increase in leakiest source-drain "surface" potential	V
$\Delta \phi_{1(sb)}$	SCE-induced change in back-surface potential	V
$\Delta \phi_{1(sf)}$	SCE-induced change in front-surface potential	V
$\Delta \Phi_{ m Gf}$	difference in front-gate work function relative to midgap	eV
$\Delta \phi^{QM}$	change in channel potential due to quantization	V
$\Delta \phi_{\rm sf}^{\rm QM}$	change in front-surface potential due to quantization	V
DIBL	drain-induced barrier lowering	mV/V
ΔQ_i^{DICE}	DICE-induced change in inversion (channel) charge density	C/cm ²
Δr^{QM}	change in charge-coupling factor due to QMEs	
Δr^{SCE}	change in charge-coupling factor due to SCEs	
ΔV_{OS}	offset voltage between front and back bias	V
ΔV_{ta}	change in V_{ta} due to stored charge in the body	V
ΔV_t^{QM}	V _t shift due to QMEs	V
ΔV_t^{SCE}	V _t shift due to SCEs	V
Δz_i	over-diffusion of source/drain junction in bulk FinFET	nm
E ₀	ground-state energy	J
Ec	Conduction-band-edge energy	J
E _{eff}	effective transverse electric field	V/cm

Er	Fermi energy level	J
E _o	energy bandgap	J
ε _{hk}	permittivity of high-k dielectric	F/cm
Ei	intrinsic Fermi level	J
E _i	ith-subband energy in unprimed valley	J
E'	ith-subband energy in primed valley	J
$E_{i(kin)}^{J}$	kinetic energy of carriers in jth subband	J
Ei(pot)	potential energy of carriers in jth subband	J
ε _{ox}	oxide permittivity	F/cm
ϵ_{Si}	silicon permittivity	F/cm
E_v	valence-band-edge energy	J
E _x	transverse electric field	V/cm
E _{xc}	weak-inversion (constant) transverse field in UTB	V/cm
E _{xsb}	transverse electric field at back surface	V/cm
E _{xsf}	transverse electric field at front surface	V/cm
Ey	lateral electric field	V/cm
Ey0	lateral electric field at virtual source at back surface	V/cm
φ	UTB potential	V
$\phi_{0(\max)}$	potential at the leakiest source-drain "surface"	V
ϕ_1	long-channel potential	V
ϕ_{B}	Fermi potential of the body	V
φ _c	band bending necessary for inversion/accumulation	V
φ ^{CL}	classical channel potential	V
Φ_{Gb}	back-gate work function	eV
Φ_{GbS}	back gate-body work-function difference	eV
$\Phi_{ m Gf}$	front-gate work function	eV
$\Phi_{ m GfS}$	tront-gate-body work-function difference	eV
t _{LO}	LO frequency	MHZ
Ψ_{MS}	gate-body work-function difference	ev
φ` £	quantum-mechanical channel potential	V MII-
I _{RF}	RF frequency	MHZ
φ _{sb}	front surface potential	V
Ψ_{sf}	front-surface potential	V
$\phi_{\rm sf}$	degree of corrier occupation of higher subhand energies	v
Ŷ	propertionality constant for SCE impact on BOX field fringing	
Ŷ	degeneracy of upprimed valley	
s r'	degeneracy of primed valley	
5 h	Planck's constant	I_s
n hai	fin height of FinFET	5-5 nm
Insi Insi	narasitic_BIT current	Δ
IBM.	MOSFET saturation current (per unit width)	A/um
IDS(sat)	generation current in the body	Δ
	impact-ionization-based generation current	Δ
I _{G1}	MOSEFT off-state current (per unit width)	A/um
-ott Lan	MOSFET on-state current (per unit width)	A/µm
-on Ip	recombination current in the body	A
k	Boltzmann constant	J/K
k	dielectric constant of high- k dielectric	
κ	proportionality constant for V_{DS} -impact on BOX field fringing	
λ	MOSFET scale/natural length	nm

List of symbols

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L _D	Debye length	nm
L _e	effective channel length with modulation	nm
L _{eD}	gate-drain underlap	nm
L _{eff}	effective channel length	nm
L _{eff(strong)}	strong-inversion effective channel length	nm
L _{eff(weak)}	weak-inversion effective channel length	nm
L _{eS}	gate-source underlap	nm
L _{eSD}	gate-source/drain underlap	nm
L _{ext}	source/drain extension length	nm
Lg	MOSFET gate length	nm
Lgch	MOSFET gradual-channel length	nm
L _{met}	MOSFET metallurgical channel length	nm
Ls	location of virtual source	nm
m ₀	free-electron mass	kg
m _d	density-of-states effective mass	kg
m _x	effective mass in confinement direction	kg
$m_{x(100)}$	m_x along {100}-Si surface	kg
$m_{x(110)}$	m_x along {110}-Si surface	kg
μ_{co}	Coulomb-limited carrier mobility	cm ² /V-s
μ_{eff}	effective carrier mobility	cm ² /V-s
μ_{max}	maximum saturation value of $\mu_{\rm ph}$	cm ² /V-s
μ_{min}	minimum saturation value of μ_{ph}	cm ² /V-s
μ ₀	constant low-field carrier mobility	cm ² /V-s
μ _{ph}	phonon-limited carrier mobility	cm ² /V-s
$\mu_{\rm ph(bulk)}$	bulk-phonon carrier mobility	cm ² /V-s
μ_{sr}	surface-roughness-limited carrier mobility	cm ² /V-s
n	electron concentration	cm^{-3}
N _{AL}	punch-through-stop doping density	cm^{-3}
N _B	doping density in the body	cm^{-3}
N _c	effective density of states in conduction band	cm^{-3}
n _i	intrinsic carrier concentration	cm^{-3}
N _{inv}	inversion-carrier density	cm^{-2}
Ni	inversion-carrier density (per unit area) in jth subband	cm^{-2}
N _{SD}	source/drain doping density	cm^{-3}
N _v	effective density of states in valence band	cm^{-3}
p	hole concentration	cm^{-3}
P	fin pitch	nm
q	electron charge	С
Qa	accumulation charge density (per unit area)	C/cm ²
Qb	depletion-charge density in body (per unit area)	C/cm ²
Q _B	body terminal charge	С
Q _D	drain terminal charge	С
Q _{Gb}	back-gate terminal charge	С
Q _{Gf}	front-gate terminal charge	С
Qi	inversion-charge density (per unit area)	C/cm ²
Q _{i0}	inversion-charge density at $V_{DS} = 0 V$	C/cm ²
Q _{ib}	bulk component of inversion-charge density	C/cm ²
Q _i ^{CL}	classical inversion-charge density	C/cm ²
Q	quantum-mechanical inversion-charge density	C/cm ²
Qis	surface component of inversion-charge density	C/cm ²
Qs	source terminal charge	С
	-	

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r	UTB-MOSFET charge-coupling factor		
r _a	charge-coupling factor for accumulated body		
r _{eff}	effective charge-coupling factor		
R _{ext}	extrinsic source/drain resistance	Ω	
R _{SD}	extrinsic source/drain series resistance	Ω	
S	inverse subthreshold slope (gate swing)	mV/dec	
$\sigma_{\rm L}$	lateral straggle of source/drain doping profile	nm	
$\sigma_{ m V}$	vertical straggle of PTS doping profile	nm	
Т	temperature	K	
t _{BOX}	BOX thickness of SOI MOSFETs	nm	
tg	gate height	nm	
t _{hk}	thickness of high-k dielectric	nm	
t _{ox}	gate-oxide thickness	nm	
t _{oxb}	back-gate oxide thickness	nm	
t _{oxf}	front-gate oxide thickness	nm	
τ_{pd}	propagation delay	ps	
t _{Si}	UTB thickness	nm	
V	carrier velocity	cm/s	
v _b	average carrier velocity in fin bulk	cm/s	
V_{bi}	built-in junction potential	V	
V_{BS}	body-source voltage	V	
V_{DD}	supply voltage	V	
V _{DS}	drain-source voltage	V	
V _{DS(eff)}	effective drain-source voltage at end of gradual chann	el V	
V _{DS(sat)}	MOSEFT drain saturation voltage	V	
V_{FB}	flat-band voltage	V	
V_{FBb}	back-gate flat-band voltage	V	
V_{FBf}	front-gate flat-band voltage	V	
V_{Gb}	back-gate voltage	V	
V_{Gb}^{A}	onset V_{GB} for back accumulation in UTB	V	
V_{Gb}^{BI}	onset V_{GB} for predominant bulk inversion in UTB	V	
V_{GB}^{I}	onset V _{GB} for back inversion in UTB	V	
V _{GbS(eff)}	effective back-gate voltage due to BOX field fringing	V	
V_{Gf}	front-gate voltage	V	
V_{GP}	ground-plane voltage	V	
V_{GS}	gate-source voltage	V	
Vs	average carrier velocity at fin surfaces	cm/s	
Vsat	saturation velocity of carriers	cm/s	
Vsat(eff)	effective saturation velocity of carriers	cm/s	
Vt	threshold voltage	V	
V _{t(ADG)}	threshold voltage of ADG MOSFET	V	
V _{t(SDG)}	threshold voltage of SDG MOSFET	V	
V _{t(thickBOX)}	threshold voltage of FD/SOI MOSFET with thick BO	X V	
V _{t(thinBOX)}	threshold voltage of FD/SOI MOSFET with thin BOX	K V	
VA	UTB-MOSFET Vt for accumulated back surface	V	
V_{tf}	threshold voltage of front surface	V	
V _{ts}	strong-inversion threshold voltage	V	
V_{tw}	weak-inversion threshold voltage	V	
W _{eff}	MOSFET effective width	nm	
W _{eff(DG)}	effective gate width of DG FinFET	nm	
W _{eff(TG)}	effective gate width of TG FinFET	nm	
511(10)			

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Wg	gate width	nm
W _{Si}	fin width of FinFET	nm
x _{av}	average inversion-carrier depth	nm
Xc	inversion-charge centroid	nm
ψ	carrier wave function (1-D)	$nm^{-1/2}$
ψ_j	carrier wave function in jth subband (1-D)	$nm^{-1/2}$

Acronyms

ADG	asymmetrical double-gate
BJT	bipolar junction transistor
BOX	buried oxide (in SOI structure)
CMOS	complementary MOS
DG	double-gate
DIBL	drain-induced barrier lowering
DICE	drain-induced charge enhancement
DOS	density of (quantum) states
DRAM	dynamic random-access memory
EOT	effective gate-oxide thickness
FD	fully depleted
GIDL	gate-induced drain leakage
GP	ground plane
HP	high performance
IC	integrated circuit
IGFET	independent-gate (DG) MOSFET
ITFET	inverted-T (hybrid) field-effect transistor
ITRS	International Technology Roadmap for Semiconductors
LP	low power
LSTP	low standby power
MOS	metal (gate)-oxide (insulator)-semiconductor
MOSFET	MOS field-effect transistor
MPU	micro-processing unit
PD	partially depleted
PE	Poisson's equation
PTS	punch-through stopping
QME	quantum-mechanical effect
QSA	quasi-static approximation
RDF	random dopant fluctuation
SCE	short-channel effect
SDE	source/drain extension
SDG	symmetrical double-gate
SG	single-gate

xvi	List of	acronyms
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SIA	Semiconductor Industry Association
SNM	static noise margin
SOI	silicon-on-insulator
SRAM	static random-access memory
TG	triple-gate
UTB	ultra-thin body
VLSI	very large-scale integration