Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs

Understand the theory, design, and applications of the two principal candidates for the next mainstream semiconductor-industry device with this concise and clear guide to FD/UTB transistors.

This book

- Describes FD/SOI MOSFETs and 3-D FinFETs in detail
- Covers short-channel effects, quantum-mechanical effects, and applications of UTB devices to floating-body DRAM and conventional SRAM
- Provides design criteria for nanoscale FinFET and nanoscale thin- and thick-BOX planar FD/SOI MOSFET to help reduce technology development time
- Projects potential nanoscale UTB CMOS performances
- Contains end-of-chapter exercises

For professional engineers in the CMOS IC field who need to know about optimal nonclassical device design and integration, this is a must-have resource.

Jerry G. Fossum is Distinguished Professor Emeritus of Electrical and Computer Engineering at the University of Florida, Gainesville, and a Fellow of the IEEE. He won the IEEE/EDS J. J. Ebers Award in 2004 for "outstanding contributions to the advancement of SOI CMOS devices and circuits through modeling."

Vishal P. Trivedi is a Member of the Technical Staff and a Distinguished Innovator at Freescale Semiconductor, Inc., and a Senior Member of the IEEE.

"The future of CMOS technology lies in replacing the classical, bulk MOSFET with new transistor structures such as the FinFET and ultra-thin body MOSFET. Those with a solid background in classical MOS device theory will find here an authoritative and comprehensive treatment of the final frontier in CMOS technology."

Mark Lundstrom, Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering, Purdue University

"A valuable volume on the design and modeling of silicon-on-insulator and multiple-gate MOSFETs by a pioneer and expert on the subject."

Yuan Taur, University of California at San Diego

"This is precisely the book everybody in the advanced nano-CMOS world wanted to see out ASAP. Timely, brilliant and most useful - written by a Master (VT) and his own former Master (JF). A life experience is condensed and distilled to provide the necessary ingredients needed for understanding the physics mechanisms and for pursuing with transistor modeling and circuit design. The book is primarily addressed to specialists, engineers and graduate students. This is not a romantic novel about SOI and FinFET affair; it is solid stuff where advanced concepts, strong affirmations and lots of practical equations do not leave space for scientific dust."

Sorin Cristoloveanu, CNRS, Grenoble, France

"This is a timely book about SOI MOSFETs and FinFETs written by one of the leading authorities in the field and his former student. Since FinFETs have started being implemented by various companies in production, there is a need for clear understanding of the design trade-offs of such devices. Prof. Fossum, who has done seminal work on modeling SOI MOSFETs since the 1980s, provides a clear elucidation of the physics of these devices. Graduate students, faculty and industrial practitioners should benefit from the pedagogy in this book."

Sanjay Banerjee, University of Texas at Austin

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Contents

Preface

The computer revolution (i.e., faster, smaller, and cheaper computers), and the technologies it has enabled (e.g., the Internet, laptops, smart phones), have been driven by continued size-scaling of the CMOS transistors in the constituent integrated circuits (ICs, e.g., the microprocessor) of the computer. This scaling, which has doubled the transistor density on the CMOS IC chip about every two years, has been achieved by simply ratioing the dimensions and related parameters of the basic, classical transistor structure (i.e., the planar single-gate MOSFET in bulk silicon or partially depleted SOI) (Taur and Ning, 2009) as improvements in lithography enabled reduced minimum feature size. The CMOS devices have now become so small (e.g., gate lengths are 30–40 nm) that this straightforward scaling is no longer possible, mainly because of fundamental limitations in reliable doping of the classical MOSFET. Thus, continued CMOS scaling will require a new, nonclassical transistor structure with ultra-thin body (UTB) that avoids these limitations. The first concrete evidence of the transition to a UTB transistor structure is Intel Corporation's adoption of the "trigate transistor" (or FinFET) (Auth *et al*., 2012) for 22 nm CMOS technology and beyond.

This book details the fundamental physics of silicon-based UTB MOSFETs, overviews their designs, with links to the process integration, and projects potential nanoscale UTB-CMOS performance. The presentations are facilitated by the authors' process/physics-based compact model for double-gate MOSFETs, UFDG (Appendix). This book is suitable as a textbook for a one-semester graduate or senior-undergraduate university course, as well as for a fundamental guide to optimal nonclassical device design and integration for professional engineers in the CMOS IC field. The prerequisites are good backgrounds in basic semiconductor device physics (e.g., as in Sze and Ng (2007)) and in fundamentals of classical bulk-Si MOSFETs (Taur and Ning, 2009). In fact, this book is intended to be a supplementary text for the latter book.

The authors acknowledge the SOI-related works of many colleagues, which provided the bases of much of this book. Special thanks are given to Professor Fossum's former Ph.D. students who so contributed: Shishir Agrawal, Duckhyun Chang, Meng-Hsueh Chiang, Jin-Young Choi, Siddharth Chouksey, Murshed Chowdhury, Lixin Ge, Keunwoo Kim, Seung-Hwan Kim, Srinath Krishnan, Hyung-Kyu Lim, Zhichao Lu, Mario Pelella, Dongwook Suh, Surya Veeraraghavan, Glenn Workman, Ji-Woon Yang, Ping Yeh, Weimin Zhang, and Zhenming Zhou; and to Leo Mathew who has provided us

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We are also grateful to our families. Professor Fossum especially thanks his wife, Mary Fossum, for unrelenting support of his "SOI obsessions." Dr. Trivedi especially thanks his parents (Pareexit and Hansa Trivedi), brother (Vaibhav), sister-in-law (Krushangi), and niece (Eesha) for their constant love, care, and support.

Physical constants

Description	Symbol	Value and unit
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	1.38×10^{-23} J/K
Vacuum permittivity	ε_0	8.85×10^{-14} F/cm
Silicon permittivity	ε_{Si}	1.04×10^{-12} F/cm
Oxide permittivity	ε_{ox}	3.45×10^{-13} F/cm
Si_3N_4 (spacer) permittivity	ε_{sp}	6.64×10^{-13} F/cm
Planck's constant	h	6.63×10^{-34} J-s
Free-electron mass	m_0	9.1×10^{-31} kg
Thermal voltage (T = 300 K)	kT/q	0.0259 V
Silicon electron affinity	χ_{Si}	4.05 eV
Silicon bandgap	$E_{g(Si)}$	1.12 eV
Silicon intrinsic carrier concentration (T = 300 K)	n_i	1.33×10^{10} cm^{-3}
Silicon effective density of states in conduction band (T = 300 K)	N_c	~2.8×10^{19} cm^{-3}
Silicon effective density of states in valence band (T = 300 K)	N_v	~1.0×10^{19} cm^{-3}

Note the values (at T = 300 K) listed for n_i, N_c, and N_v. There is inconsistency in the archival literature among these constants. The given value for n_i, which is lower than commonly presumed (Taur and Ning, 2009), was taken from unpublished measurements done by C. T. Sah *et al*. in 1974 at the University of Illinois; correspondingly, $E_{g(Si)}$ was measured at 1.12 eV, which is the commonly accepted value. The given values for N_c and N_v, which are common, are indicated to be crude approximations because they are not consistent with n_i and $E_{g(Si)}$ in the parabolic band-based expression for $n_i(E_g, N_c, N_v, T)$ (Taur and Ning, 2009).

Symbols

a_f	FinFET fin aspect ratio	
β	coefficient for surface-roughness-limited mobility model	V^3/cm^3-s
β	term in C_{ifw} model	radian
b_j	variational parameter of jth subband	
b_0	variational parameter of ground-state subband	
χ_{Si}	electron affinity	eV
C_b	body capacitance (per unit area)	F/cm^2
C_B	composite body capacitance	F
$C_{b(eff)}$	effective body capacitance (per unit area)	F/cm^2
C_{bf}	BOX fringe capacitance (per unit width)	F/cm
C_d	depletion capacitance (per unit area)	F/cm^2
C_G	MOSFET gate capacitance (per unit area)	F/cm^2
C_i	inversion-layer capacitance (per unit area)	F/cm^2
C_{if}	inner-fringe capacitance (per unit width)	F/cm
C_{of}	outer-fringe capacitance (per unit width)	F/cm
C_{ox}	gate-oxide capacitance (per unit area)	F/cm^2
C_{oxb}	back-gate oxide capacitance (per unit area)	F/cm^2
C_{oxf}	front-gate oxide capacitance (per unit area)	F/cm^2
$C_{S/D}$	source/drain-junction capacitance (per unit area)	F/cm^2
$\Delta\phi_0$	drain bias-induced increase in channel potential	V
$\Delta\phi_{0(sb)}$	drain bias-induced increase in back-surface potential	V
$\Delta\phi_{0(sf)}$	drain bias-induced increase in front-surface potential	V
$\Delta\phi_{1(max)}$	increase in leakiest source-drain "surface" potential	V
$\Delta\phi_{1(sb)}$	SCE-induced change in back-surface potential	V
$\Delta\phi_{1(sf)}$	SCE-induced change in front-surface potential	V
$\Delta\Phi_{Gf}$	difference in front-gate work function relative to midgap	eV
$\Delta\phi^{QM}$	change in channel potential due to quantization	V
$\Delta\phi_{sf}^{QM}$	change in front-surface potential due to quantization	V
DIBL	drain-induced barrier lowering	mV/V
ΔQ_i^{DICE}	DICE-induced change in inversion (channel) charge density	C/cm^2
Δr^{QM}	change in charge-coupling factor due to QMEs	
Δr^{SCE}	change in charge-coupling factor due to SCEs	
ΔV_{OS}	offset voltage between front and back bias	V
ΔV_{ta}	change in V_{ta} due to stored charge in the body	V
ΔV_t^{QM}	V_t shift due to QMEs	V
ΔV_t^{SCE}	V_t shift due to SCEs	V
Δz_j	over-diffusion of source/drain junction in bulk FinFET	nm
E_0	ground-state energy	J
E_c	Conduction-band-edge energy	J
E_{eff}	effective transverse electric field	V/cm

E_F	Fermi energy level	J
E_g	energy bandgap	J
ε_{hk}	permittivity of high-*k* dielectric	F/cm
E_i	intrinsic Fermi level	J
E_j	jth-subband energy in unprimed valley	J
E_j'	jth-subband energy in primed valley	J
$E_{j\langle kin\rangle}$	kinetic energy of carriers in jth subband	J
$E_{j\langle pot\rangle}$	potential energy of carriers in jth subband	J
ε_{ox}	oxide permittivity	F/cm
ε_{Si}	silicon permittivity	F/cm
E_v	valence-band-edge energy	J
E_x	transverse electric field	V/cm
E_{xc}	weak-inversion (constant) transverse field in UTB	V/cm
E_{xsb}	transverse electric field at back surface	V/cm
E_{xsf}	transverse electric field at front surface	V/cm
E_y	lateral electric field	V/cm
E_{y0}	lateral electric field at virtual source at back surface	V/cm
ϕ	UTB potential	V
$\phi_{0(max)}$	potential at the leakiest source-drain "surface"	V
ϕ_1	long-channel potential	V
ϕ_B	Fermi potential of the body	V
ϕ_c	band bending necessary for inversion/accumulation	V
ϕ^{CL}	classical channel potential	V
Φ_{Gb}	back-gate work function	eV
Φ_{GbS}	back gate-body work-function difference	eV
Φ_{Gf}	front-gate work function	eV
Φ_{GfS}	front-gate-body work-function difference	eV
f_{LO}	LO frequency	MHz
Φ_{MS}	gate-body work-function difference	eV
ϕ^{QM}	quantum-mechanical channel potential	V
f_{RF}	RF frequency	MHz
ϕ_{sb}	back-surface potential	V
ϕ_{sf}	front-surface potential	V
ϕ_{sf}^t	front-surface potential at threshold	V
γ	degree of carrier occupation of higher subband energies	
γ	proportionality constant for SCE-impact on BOX field fringing	
g	degeneracy of unprimed valley	
g′	degeneracy of primed valley	
h	Planck's constant	J-s
h_{Si}	fin height of FinFET	nm
I_{BJT}	parasitic-BJT current	A
$I_{DS(sat)}$	MOSFET saturation current (per unit width)	A/μm
I_G	generation current in the body	A
I_{Gi}	impact-ionization-based generation current	A
I_{off}	MOSFET off-state current (per unit width)	A/μm
I_{on}	MOSFET on-state current (per unit width)	A/μm
I_R	recombination current in the body	A
k	Boltzmann constant	J/K
k	dielectric constant of high-*k* dielectric	
κ	proportionality constant for V_{DS}-impact on BOX field fringing	
λ	MOSFET scale/natural length	nm

L_D	Debye length	nm
L_e	effective channel length with modulation	nm
L_{eD}	gate-drain underlap	nm
L_{eff}	effective channel length	nm
$L_{eff(strong)}$	strong-inversion effective channel length	nm
$L_{eff(weak)}$	weak-inversion effective channel length	nm
L_{eS}	gate-source underlap	nm
L_{eSD}	gate-source/drain underlap	nm
L_{ext}	source/drain extension length	nm
L_g	MOSFET gate length	nm
L_{gch}	MOSFET gradual-channel length	nm
L_{met}	MOSFET metallurgical channel length	nm
L_s	location of virtual source	nm
m_0	free-electron mass	kg
m_d	density-of-states effective mass	kg
m_x	effective mass in confinement direction	kg
$m_{x\langle 100\rangle}$	m_x along {100}-Si surface	kg
$m_{x\langle 110\rangle}$	m_x along {110}-Si surface	kg
μ_{co}	Coulomb-limited carrier mobility	$cm^2/V\text{-}s$
μ_{eff}	effective carrier mobility	$cm^2/V\text{-}s$
μ_{max}	maximum saturation value of μ_{ph}	$cm^2/V\text{-}s$
μ_{min}	minimum saturation value of μ_{ph}	$cm^2/V\text{-}s$
μ_0	constant low-field carrier mobility	$cm^2/V\text{-}s$
μ_{ph}	phonon-limited carrier mobility	$cm^2/V\text{-}s$
$\mu_{ph(bulk)}$	bulk-phonon carrier mobility	$cm^2/V\text{-}s$
μ_{sr}	surface-roughness-limited carrier mobility	$cm^2/V\text{-}s$
n	electron concentration	cm^{-3}
N_{AL}	punch-through-stop doping density	cm^{-3}
N_B	doping density in the body	cm^{-3}
N_c	effective density of states in conduction band	cm^{-3}
n_i	intrinsic carrier concentration	cm^{-3}
N_{inv}	inversion-carrier density	cm^{-2}
N_j	inversion-carrier density (per unit area) in jth subband	cm^{-2}
N_{SD}	source/drain doping density	cm^{-3}
N_v	effective density of states in valence band	cm^{-3}
p	hole concentration	cm^{-3}
P	fin pitch	nm
q	electron charge	C
Q_a	accumulation charge density (per unit area)	C/cm^2
Q_b	depletion-charge density in body (per unit area)	C/cm^2
Q_B	body terminal charge	C
Q_D	drain terminal charge	C
Q_{Gb}	back-gate terminal charge	C
Q_{Gf}	front-gate terminal charge	C
Q_i	inversion-charge density (per unit area)	C/cm^2
Q_{i0}	inversion-charge density at $V_{DS} = 0$ V	C/cm^2
Q_{ib}	bulk component of inversion-charge density	C/cm^2
Q_i^{CL}	classical inversion-charge density	C/cm^2
Q_i^{QM}	quantum-mechanical inversion-charge density	C/cm^2
Q_{is}	surface component of inversion-charge density	C/cm^2
Q_S	source terminal charge	C

r	UTB-MOSFET charge-coupling factor	
r_a	charge-coupling factor for accumulated body	
r_{eff}	effective charge-coupling factor	
R_{ext}	extrinsic source/drain resistance	Ω
R_{SD}	extrinsic source/drain series resistance	Ω
S	inverse subthreshold slope (gate swing)	mV/dec
σ_L	lateral straggle of source/drain doping profile	nm
σ_V	vertical straggle of PTS doping profile	nm
T	temperature	K
t_{BOX}	BOX thickness of SOI MOSFETs	nm
t_g	gate height	nm
t_{hk}	thickness of high-k dielectric	nm
t_{ox}	gate-oxide thickness	nm
t_{oxb}	back-gate oxide thickness	nm
t_{oxf}	front-gate oxide thickness	nm
τ_{pd}	propagation delay	ps
t_{Si}	UTB thickness	nm
v	carrier velocity	cm/s
v_b	average carrier velocity in fin bulk	cm/s
V_{bi}	built-in junction potential	V
V_{BS}	body-source voltage	V
V_{DD}	supply voltage	V
V_{DS}	drain-source voltage	V
$V_{DS(eff)}$	effective drain-source voltage at end of gradual channel	V
$V_{DS(sat)}$	MOSEFT drain saturation voltage	V
V_{FB}	flat-band voltage	V
V_{FBb}	back-gate flat-band voltage	V
V_{FBf}	front-gate flat-band voltage	V
V_{Gb}	back-gate voltage	V
V_{Gb}^{A}	onset V_{GB} for back accumulation in UTB	V
V_{Gb}^{BI}	onset V_{GB} for predominant bulk inversion in UTB	V
V_{GB}^{I}	onset V_{GB} for back inversion in UTB	V
$V_{GbS(eff)}$	effective back-gate voltage due to BOX field fringing	V
V_{Gf}	front-gate voltage	V
V_{GP}	ground-plane voltage	V
V_{GS}	gate-source voltage	V
v_s	average carrier velocity at fin surfaces	cm/s
v_{sat}	saturation velocity of carriers	cm/s
$v_{sat(eff)}$	effective saturation velocity of carriers	cm/s
V_t	threshold voltage	V
$V_{t(ADG)}$	threshold voltage of ADG MOSFET	V
$V_{t(SDG)}$	threshold voltage of SDG MOSFET	V
$V_{t(thickBOX)}$	threshold voltage of FD/SOI MOSFET with thick BOX	V
$V_{t(thinBOX)}$	threshold voltage of FD/SOI MOSFET with thin BOX	V
V_t^A	UTB-MOSFET V_t for accumulated back surface	V
V_{tf}	threshold voltage of front surface	V
V_{ts}	strong-inversion threshold voltage	V
V_{tw}	weak-inversion threshold voltage	V
W_{eff}	MOSFET effective width	nm
$W_{eff(DG)}$	effective gate width of DG FinFET	nm
$W_{eff(TG)}$	effective gate width of TG FinFET	nm

W_g	gate width	nm
w_{Si}	fin width of FinFET	nm
x_{av}	average inversion-carrier depth	nm
x_c	inversion-charge centroid	nm
ψ	carrier wave function (1-D)	$nm^{-1/2}$
ψ_j	carrier wave function in jth subband (1-D)	$nm^{-1/2}$

Acronyms

ADG	asymmetrical double-gate
BJT	bipolar junction transistor
BOX	buried oxide (in SOI structure)
CMOS	complementary MOS
DG	double-gate
DIBL	drain-induced barrier lowering
DICE	drain-induced charge enhancement
DOS	density of (quantum) states
DRAM	dynamic random-access memory
EOT	effective gate-oxide thickness
FD	fully depleted
GIDL	gate-induced drain leakage
GP	ground plane
HP	high performance
IC	integrated circuit
IGFET	independent-gate (DG) MOSFET
ITFET	inverted-T (hybrid) field-effect transistor
ITRS	International Technology Roadmap for Semiconductors
LP	low power
LSTP	low standby power
MOS	metal (gate)-oxide (insulator)-semiconductor
MOSFET	MOS field-effect transistor
MPU	micro-processing unit
PD	partially depleted
PE	Poisson's equation
PTS	punch-through stopping
QME	quantum-mechanical effect
QSA	quasi-static approximation
RDF	random dopant fluctuation
SCE	short-channel effect
SDE	source/drain extension
SDG	symmetrical double-gate
SG	single-gate

SIA	Semiconductor Industry Association
SNM	static noise margin
SOI	silicon-on-insulator
SRAM	static random-access memory
TG	triple-gate
UTB	ultra-thin body
VLSI	very large-scale integration