

Contents

List of Algorithms	<i>page</i> xi
Preface	xiii

PART I: PRELIMINARIES

1 Sets and Functions	3
1.1 Sets	3
1.2 Relations and Functions	9
1.3 Boolean Functions	13
1.4 Commutative and Associative Binary Operations	15
2 Induction and Recursion	19
2.1 Induction	19
2.2 Recursion	23
2.3 Application: One-to-One and Onto Functions	24
3 Sequences and Series	29
3.1 Sequences	29
3.2 Series	31
4 Directed Graphs	38
4.1 Definitions	38
4.2 Topological Ordering	41
4.3 Longest Path in a DAG	43
4.4 Rooted Trees	47
5 Binary Representation	52
5.1 Division and Modulo	52
5.2 Bits and Strings	53
5.3 Bit Ordering	54
5.4 Binary Representation	55
5.5 Computing a Binary Representation	58
5.6* More on Unique Binary Representation	65

6 Propositional Logic	68
6.1 Boolean Formulas	68
6.2 Truth Assignments	73
6.3 Satisfiability and Logical Equivalence	73
6.4 Interpreting a Boolean Formula as a Function	76
6.5 Substitution	80
6.6 Complete Sets of Connectives	82
6.7 Important Tautologies	86
6.8 De Morgan's Laws	88
7 Asymptotics	94
7.1 Order of Growth Rates	94
7.2 Recurrence Equations	98
8* Computer Stories: Big Endian versus Little Endian	104

PART II: COMBINATIONAL CIRCUITS

9 Representations of Boolean Functions by Formulas	109
9.1 Sum of Products	109
9.2 Product of Sums	113
9.3 The Finite Field $GF(2)$	115
9.4 Satisfiability	119
9.5 Relation to P versus NP	119
9.6* Minimization Heuristics	120
10* The Digital Abstraction	133
10.1 Transistors	133
10.2 A CMOS Inverter	135
10.3 From Analog Signals to Digital Signals	136
10.4 Transfer Functions of Gates	138
10.5 The Bounded-Noise Model	140
10.6 The Digital Abstraction in the Presence of Noise	141
10.7 Stable Signals	143
10.8 Summary	143
11 Foundations of Combinational Circuits	145
11.1 Combinational Gates: An Analog Approach	145
11.2 Back to the Digital World	147
11.3 Combinational Gates	149
11.4 Wires and Nets	150
11.5 Combinational Circuits	152
11.6 Properties of Combinational Circuits	156
11.7 Simulation and Delay Analysis	156
11.8 Completeness	160
11.9 Cost and Propagation Delay	164

Contents vii

11.10 Example: Relative Gate Costs and Delay	165
11.11 Semantics and Syntax	165
11.12 Summary	166
12 Trees	168
12.1 Associative Boolean Functions	168
12.2 Trees of Associative Boolean Gates	170
12.3 Optimality of Trees	175
12.4 Summary	182
13 Decoders and Encoders	184
13.1 Buses	184
13.2 Decoders	186
13.3 Encoders	192
13.4 Summary	199
14 Selectors and Shifters	201
14.1 Multiplexers	201
14.2 Cyclic Shifters	205
14.3 Logical Shifters	209
14.4 Arithmetic Shifters	211
14.5 Summary	213
15 Addition	215
15.1 Definition of a Binary Adder	215
15.2 Ripple Carry Adder	216
15.3 Lower Bounds	218
15.4 Conditional Sum Adder	220
15.5 Compound Adder	222
15.6 Reductions between Sum and Carry Bits	224
15.7 Redundant and Nonredundant Representation	225
15.8 Summary	226
16 Signed Addition	228
16.1 Representation of Negative Integers	228
16.2 Computing a Two's Complement Representation	229
16.3 Negation in Two's Complement Representation	231
16.4 Properties of Two's Complement Representation	232
16.5 Reduction: Two's Complement Addition to Binary Addition	234
16.6 A Two's-Complement Adder	238
16.7 A Two's Complement Adder/Subtractor	239
16.8 Summary	240
PART III: SYNCHRONOUS CIRCUITS	
17 Flip-Flops	247
17.1 The Clock	247

17.2	Edge-Triggered Flip-Flop	249
17.3*	Arbitration	250
17.4*	Arbiters: An Impossibility Result	251
17.5*	Necessity of Critical Segments	253
17.6	A Timing Example	255
17.7	Bounding Instability	257
17.8	Other Types of Memory Devices	258
17.9	Summary	261
18	Memory Modules	264
18.1	The Zero Delay Model	264
18.2	Registers	265
18.3	Random Access Memory (RAM)	267
18.4	Read-Only Memory (ROM)	270
18.5	Summary	271
19	Foundations of Synchronous Circuits	272
19.1	Definition	272
19.2	The Canonic Form of a Synchronous Circuit	274
19.3	Timing Analysis: The Canonic Form	275
19.4	Functionality: The Canonic Form	281
19.5	Finite State Machines	282
19.6	Timing Analysis: The General Case	283
19.7	Simulation of Synchronous Circuits	288
19.8	Synthesis and Analysis	289
19.9	Summary	290
20	Synchronous Modules: Analysis and Synthesis	294
20.1	Example: A Two-State FSM	294
20.2	Sequential Adder	296
20.3	Initialization and the Corresponding FSM	298
20.4	Counter	299
20.5	Revisiting Shift Registers	301
20.6	Revisiting RAM	302
PART IV: A SIMPLIFIED DLX		
21	The ISA of a Simplified DLX	309
21.1	Why Use Abstractions?	309
21.2	Instruction Set Architecture	310
21.3	Examples of Program Segments	318
21.4	Summary	320
22	A Simplified DLX: Implementation	323
22.1	Datapath	323
22.2	Control	330
22.3	RTL Instructions	335

Contents	ix
-----------------	-----------

22.4 Examples of Instruction Execution	336
22.5 Summary	337
Bibliography	343
Index	345