1
Introduction

1.1 Overview of MEMS fabrication

Microelectromechanical systems (MEMS) fabrication developed out of the thin-film processes first used for semiconductor fabrication. To understand the unique features of the MEMS fabrication process it is helpful to consider the semiconductor fabrication process.

The semiconductor fabrication process is cyclic. (a) First, a thin film is deposited on the wafer surface using thin-film deposition techniques. (b) A uniform photosensitive polymer (photoresist) is then deposited and (c) exposed to light from a mask that contains the pattern that is desired on the thin film. (d) The photoresist is developed to obtain the desired pattern. (e) The pattern in the photoresist is then transferred to the thin film using an etching technique, and the photoresist is removed. Figure 1.1 shows a cross section of the wafer at each step. This cycle is repeated for each new layer, with some processes requiring as many as 20 to 30 cycles.

The typical thin films that are deposited include semiconductors (e.g., polysilicon), insulators (e.g., silicon nitride), and metals (e.g., aluminum). In addition, some layers are grown (oxide), diffused, or implanted (dopants) rather than deposited using thin-film techniques. A cross section of a complementary metal oxide semiconductor (CMOS) process that includes six levels of metal is shown in Figure 1.2 [1]. A schematic diagram of one of the first MEMS devices, which used semiconductor processing for fabrication, the resonant gate transistor, is shown in Figure 1.3 [2].

The MEMS fabrication cycle, as shown in Figure 1.4, also includes thin-film deposition and patterning, but typically the films are thicker than the films used in microelectronics, the etching is deeper, and the

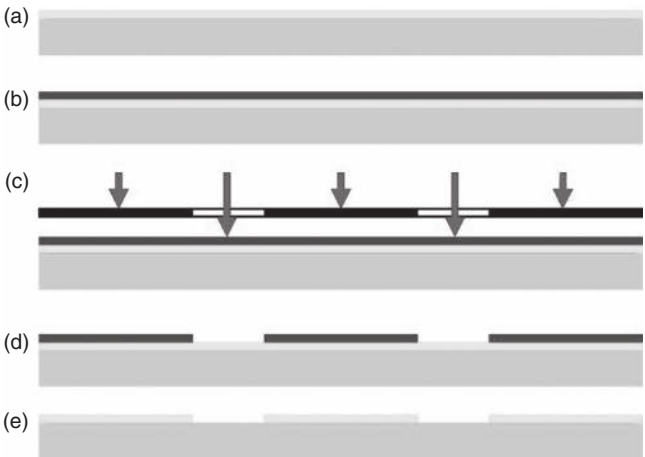

Figure 1.1 The semiconductor fabrication process. (a) Thin-film deposition (yellow), (b) photoresist deposition (blue), (c) photolithography (mask clear and opaque; red arrows), (d) photoresist development, and (e) etching to transfer the pattern in the photoresist into the thin film. See color plate section.

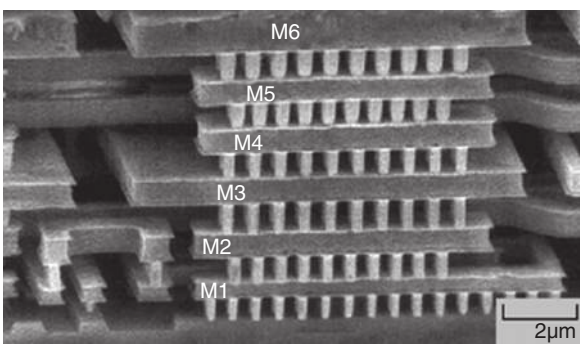

Figure 1.2 A cross-section scanning electron microscope image of a six-level metal backend structure. The insulating layers between the metal layers have been etched away, similar to the sacrificial etch that is used to release structures in the polysilicon surface micromachining process described below. (Reprinted with permission from JOM Journal of the Minerals, Metals and Materials Society.)

photolithography is more challenging because the topography from the patterning is greater [3]. The films and etches can be several microns deep, leading to topography approaching 10 μm after seven or eight layers have been deposited and patterned. Another difference is

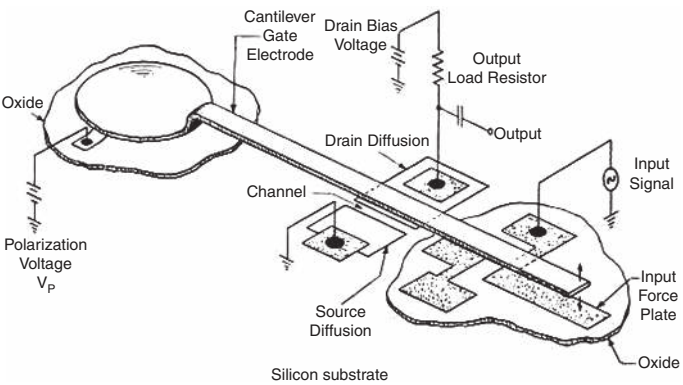

Figure 1.3 The resonant gate field effect transistor, one of the first MEMS devices. A released metal cantilever beam forms the gate electrode over the diffused source–drain channel. The input signal is applied to the input force plate, which causes the cantilever beam to vibrate, modulating the current through the transistor. Maximum vibration occurs at the resonant frequency of the cantilever beam, enabling the device to act as a high-Q electromechanical filter. (Reprinted with permission from IEEE Trans. Electron Devices, *The resonant gate transistor*, H.C. Nathanson, W.E. Newell, R.A. Wickstrom and J.R. Davis Jr., ©1967 IEEE.)

that the MEMS fabrication process ends with the release of mechanical elements such as beams and membranes. Since some elements are released, the mechanical properties of the deposited films must be controlled to avoid distortion of the released elements as they relax under the influence of residual stress and stress-gradients, as shown in Figures 1.5 and 1.6.

Controlling the mechanical properties of thin films can require considerable process development. The mechanical properties are sensitive to how the layers are deposited, what layers they are deposited on, what layers are deposited on them, and the thermal history that the layers are subjected to. As an example, each film has a unique coefficient of thermal expansion (CTE). During a typical thin-film deposition step, the wafer may be heated by hundreds of degrees. When the wafer is cooled the deposited film will have a different rate of dimensional change than the substrate, leading to a buildup of stress.

Typically each new MEMS device requires the development of a new MEMS fabrication process, so controlling the thin-film properties in one process does not necessarily help with control of the thin-film properties

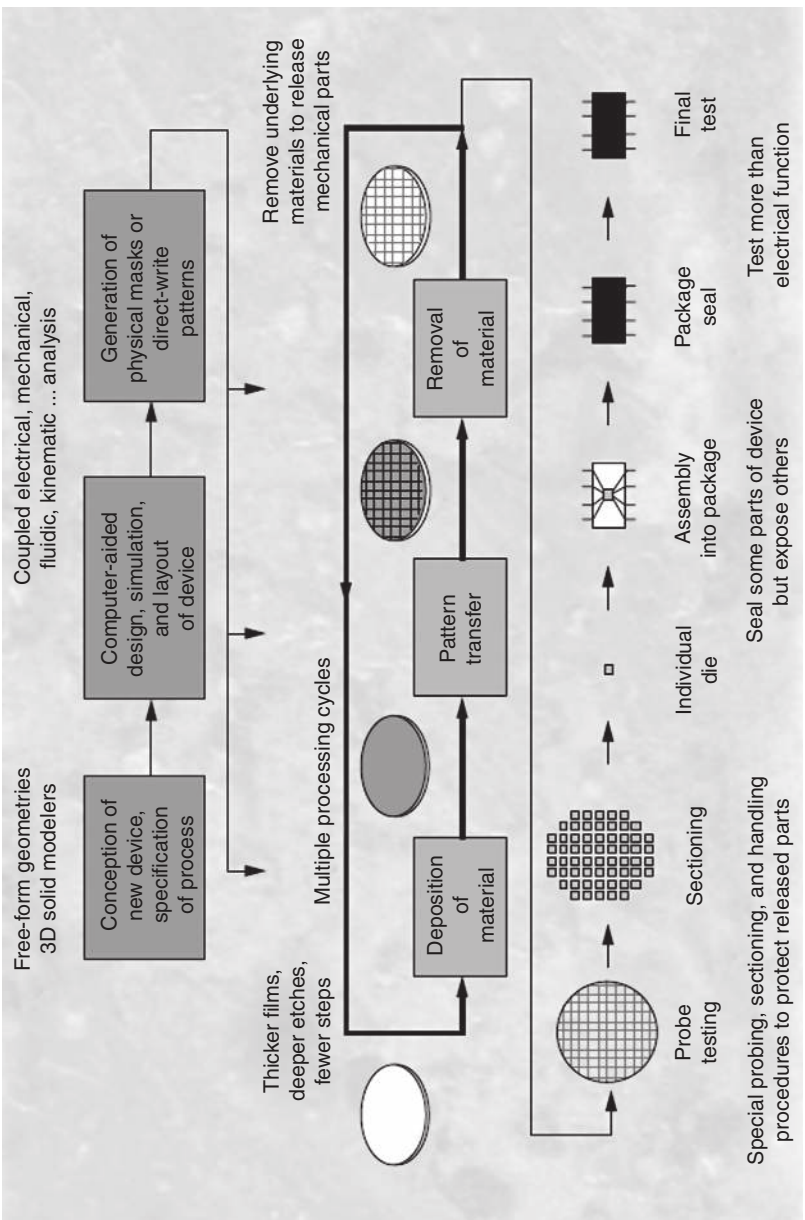

Figure 1.4

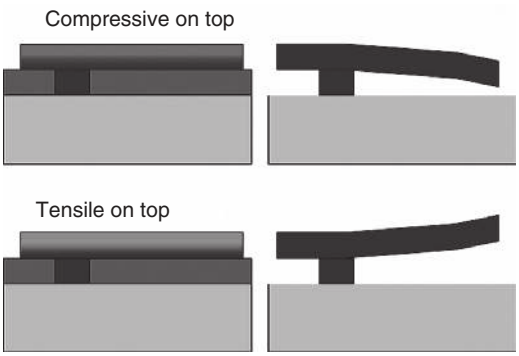

Figure 1.5 Deformation of released structures due to residual stress-gradients. In the top figure the stress is compressive on top, resulting in a downward deflection on release. In the bottom figure the film is tensile on top, resulting in an upward deflection on release. See color plate section.

in a different process. This is in contrast to the control of electrical properties in microelectronics fabrication. Here results from one process, such as the controlled doping of silicon by diffusion or implantation, can be re-applied to a different process. The development of a new MEMS process can take decades and cost millions of dollars, so it can be justified only by market demand for the MEMS device that is eventually manufactured. Here we consider some standard MEMS processes that can be used at the prototyping stage and eventually modified as required to reach the manufacturing stage.

Figure 1.4 The MEMS prototyping cycle. Once a MEMS device has been conceived and a fabrication process specified, it is modeled to the first order analytically and, if required, to a higher order using computer-aided design tools capable of coupled domain analysis (e.g., electrical, mechanical, fluidic, thermal). The design is then finalized and a layout is generated using a layout editor that creates files (GDSII or CIF) that are used to define the physical mask layers. Once the masks have been written they are used to pattern the various layers of the MEMS device in multiple processing cycles. A typical MEMS process might involve eight deposition and patterning cycles. Typically the deposited layers are thicker, and the etches deeper, than those used in integrated circuit fabrication. After all of the layers are deposited and patterned, the wafer is tested, diced (sectioned), and packaged. The sacrificial layers can be removed at either the wafer or the die level. (Reprinted with permission from IEEE Trans. Electron Devices, *MEMS: The systems function revolution*, Karen W. Markus and Kaigham J. Gabriel, ©1967 IEEE.)

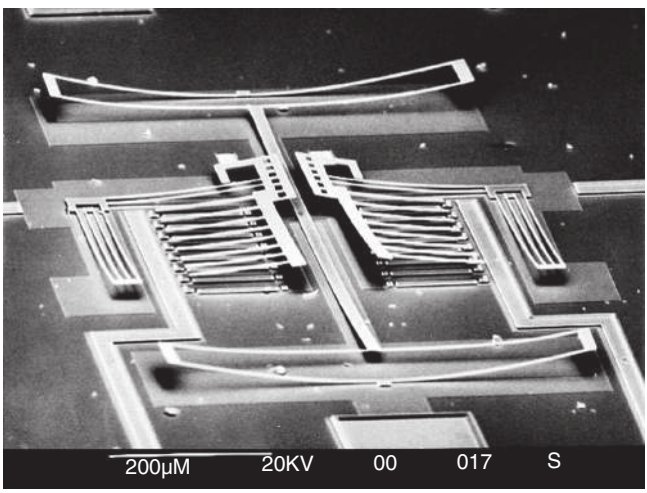

Figure 1.6 Deformation of a released structure due to stress-gradients at MCNC circa 1996. The residual stress is tensile on top of the polysilicon, causing the released structure to bend away from the substrate after release. In general, the polysilicon from MCNC was quite flat, but in this case an anneal of the sacrificial doped oxide (PSG) was left out, resulting in residual stress-gradients. (Reprinted with permission of Kristofer S.J. Pister, Berkeley Sensor and Actuator Center, UC Berkeley.)

1.2 Shared wafer processes

1.2.1 Multiproject wafer processes

There are a number of multiproject wafer (MPW) processes that are available that use bulk and surface micromachining as well as electroplating and wafer bonding. By using a robust MPW process that has stable thin-film parameters and a well-developed set of design rules, the prototyping challenges associated with process development can be avoided so that the focus of the effort can be on the MEMS design. Additional benefits are the decreased costs, because the wafer is shared between many users, and a path-to-the-sea for product manufacturing, because a commercial foundry is involved from the start, providing a low-cost proof of concept to high-volume manufacturing. A price that must be paid is that the process is already defined and cannot be altered. The only layers that are available are the layers that are used in the MPW process. Even the layer thickness cannot be altered. Nonetheless, if a standard MPW process is initially used, the foundry that provides the standard process can usually

provide minor changes such as the addition of a new layer or a change to the thickness of an existing layer at the expense of higher fabrication costs.

1.2.1.1 Surface micromachining

There are a number of surface micromachining MPW processes available that include variations in the numbers of layers as well as different layer materials. The earliest MPW surface micromachining process offered was the three-layer polysilicon surface micromachining process initially developed at UC Berkeley by Roger Howe and Richard Muller [4]. This process has been reviewed by Bustillo et al. [5]. A cross-sectional diagram of the layer stack that is currently offered by MEMSCAP in their PolyMUMPS process is shown in Figure 1.7 [6].

In this process, as shown step-by-step in cross section in Figure 1.7, the surface of a 150 mm substrate (n-type, 1–2 Ωcm) is heavily doped with phosphorus to a resistance of 10 Ω/□ to avoid charge buildup at the substrate–nitride interface when high voltages are applied between the substrate and the subsequent conducting layers. The surface is protected by a blanket low-pressure chemical vapor deposition (LPCVD) of a 0.6 μm thick insulating silicon nitride (90 MPa residual tensile stress). A 0.5 μm thick layer of LPCVD polysilicon (n-type, 30Ω/□, −25 MPa residual compressive stress) Poly0 is deposited and then patterned. This layer is typically used as a ground plane or counter-electrode and is not released. The next layer is the first oxide layer. It is a 2 μm thick phospho-silicate glass (PSG) that is deposited by LPCVD. This "sacrificial" oxide has a fast etch rate in 49% buffered hydrofluoric acid (HF) that allows for a quick release (2.5 min) of nonsacrificial (i.e., not etched by HF) "structural" layers deposited on top of it if properly spaced etch holes are included in the structural layers, as explained later. The PSG layer is also used as a solid source for phosphorus doping of the polysilicon layers that are in contact with it during the thermal anneal step used to control the level of stress in the polysilicon.

Shallow holes, approximately 0.75 μm deep, which do not go all the way through the 2 μm thick oxide, are defined using the DIMPLE mask. These "dimple" holes are later filled in with Poly1 to form tiny stalactites that hang down from the bottom of Poly1 to limit the amount of surface area contact between Poly1 and Poly0. Surface forces such as van der Waals and capillarity dominate on a microscale, which can lead to surfaces sticking together. This is so prevalent in microelectromechanical

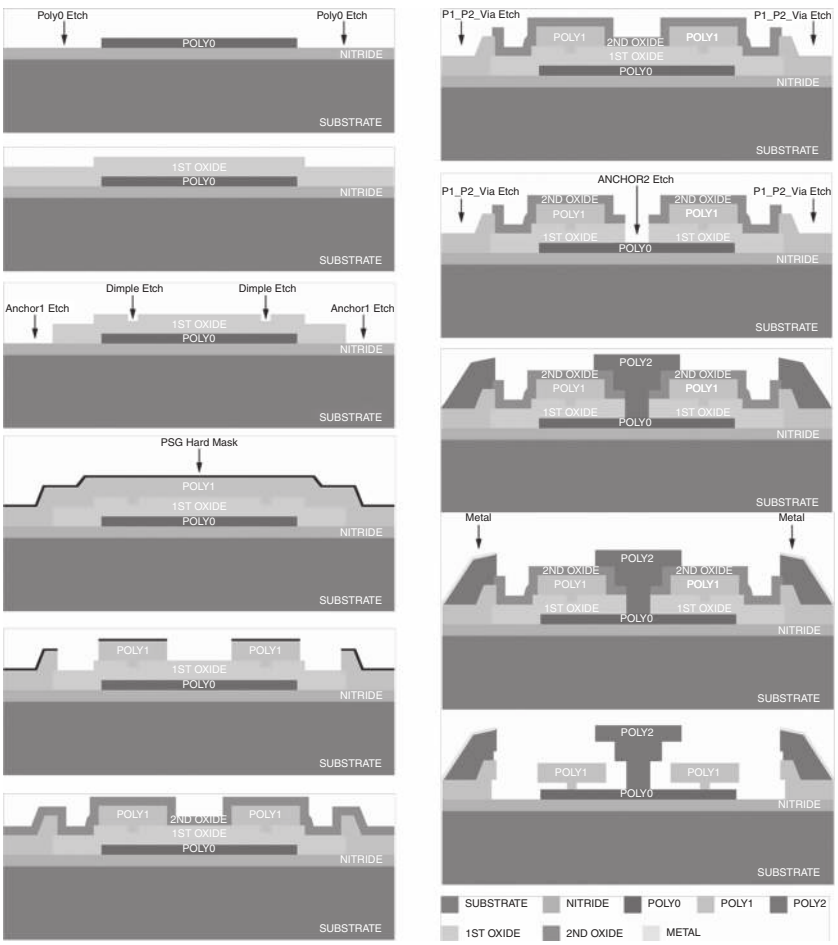

Figure 1.7 PolyMUMPS three-layer polysilicon surface micromachining process offered by MEMSCAP. Polysilicon and oxide layers are deposited and patterned in a cyclic process, with anneal steps of the doped sacrificial oxide between polysilicon depositions. Poly0 is an electrical layer that is not released. Poly1 and Poly2 are structural layers that can be released. The deposition and patterning steps shown here result in a polysilicon wheel defined in Poly1 that is constrained by a hub defined in Poly2. Dimples defined in POLY1 keep the wheel from becoming stuck to the Poly0 layer. (Reprinted with permission from MEMSCAP Inc.) See color plate section.

systems that a new term has been created – "stiction." A recommendation is to include as many dimples as the design allows. One way to make sure dimples are widespread is to include them between every release etch hole, which are spaced every 30 μm, as will be described later.

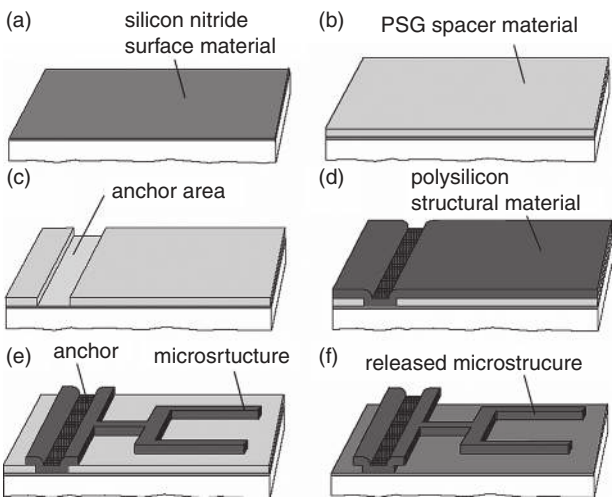

Figure 1.8 Polysilicon surface micromachining. (a) An insulating surface layer such as silicon nitride is deposited on the substrate. (b) A sacrificial spacer layer, such as phospho-silicate glass (PSG), which can be etched quickly, is deposited. (c) A hole is cut through the sacrificial layer to the insulating layer, where the structure is to be anchored to the underlying surface material. (d) The structural layer, in this example polysilicon, is then deposited. The deposition is conformal and fills in the hole that had previously been cut through the sacrificial layer. (e) The structural layer is patterned and then (f) released. (Reprinted with permission from ITC International Test Conference, MEMS Fabrication, Gary K. Fedder, ©1967 IEEE.)

Holes are next cut all the way through the first oxide layer (ANCHOR1) to anchor structures defined in Poly1 to the substrate after the PSG sacrificial spacer layer has been etched. An example is shown in Figure 1.8 [7]. Note that the polysilicon is a conformal coating, so that topographic features, such as the anchor holes, are replicated in the layers deposited on top of them. This replication of topography can give rise to mechanical interferences for features defined in the overlayers.

A common mistake made by those who are first learning to use a surface micromachining process is to leave out anchors. Since you must specify where a hole in this layer is to be placed, it is easy to leave out the anchor hole. If no anchor hole is specified, the polysilicon that is deposited over the oxide will be released during the sacrificial etch and float away. A good practice to avoid this common mistake is to take cross sections of the thin-film stack to make sure that all structures are anchored. An example of a bond pad that was not anchored and was released during the sacrificial etch is shown in Figure 1.9.

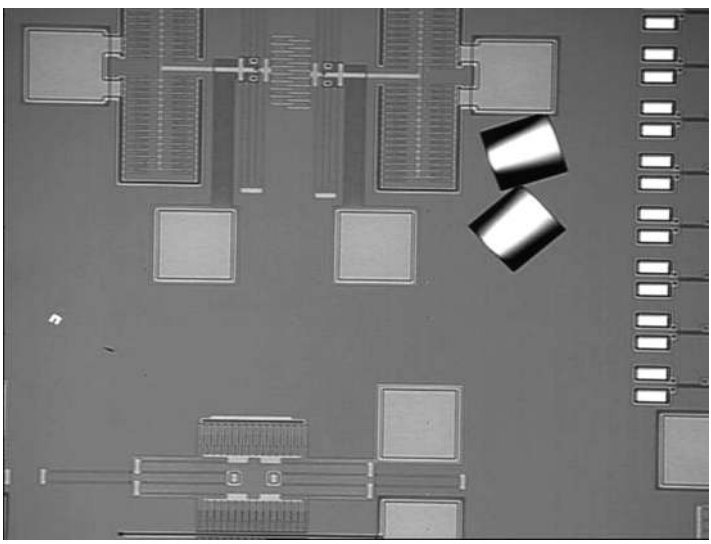

Figure 1.9 Bond pads that were not anchored are released after the sacrificial etch. Not only does this make electrical testing difficult, but the bond pads usually end up in places you do not want them. Your neighbors on a multiproject chip will be particularly annoyed if your parts land in their area! The parts that do not get stuck to the chip are often observed as "floaters" in the etch bath that is used for the sacrificial release.

After the ANCHOR1 holes have been etched, the first layer of structural polysilicon that can be released, Poly1, is deposited and patterned on top of Oxide1. This layer of polysilicon is 2 μm thick. A thin film of PSG (0.2 μm) is deposited on top of Poly1 to act as a solid source for doping the top side of the polysilicon layer, and as a hard mask for subsequent patterning of the layer. The wafer is then annealed at a high temperature (1050°C) for an hour to relieve residual stress and to dope the polysilicon. This high-temperature anneal leads to a low compressive residual stress (−10 MPa) and a resistance of 10 Ω/□. The polysilicon layer is doped from both the top and the bottom of the thin film simultaneously to minimize stress-gradients through the thickness of the thin film. A stress-gradient is a difference in stress between the top and the bottom layers of a thin film, and it can cause released structures to deform to relieve the stress. A stress-gradient that is compressive on the top causes a released structure to bend down toward the substrate, as shown in Figure 1.5. A thin film that is tensile on top causes the release structure to bend upward, away from the substrate. An example of deformations caused due to stress-gradients in the early days of PolyMUMPS process