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A transistor-level, design-intensive overview of high-speed and high-frequency monolithic integrated circuits for wireless and broadband systems from 2GHz to 200GHz, this comprehensive text covers high-speed, RF, mm-wave, and optical fiber circuits using nanoscale CMOS, SiGe BiCMOS, and III-V technologies. Step-by-step design methodologies, end-of-chapter problems, and practical simulation and design projects are provided, making this an ideal resource for senior undergraduate and graduate courses in circuit design. With an emphasis on device—circuit topology interaction and optimization, it gives circuit designers and students alike an in-depth understanding of device structures and process limitations affecting circuit performance, and is accompanied online by supporting lecture slides, student lab assignments and project descriptions, and solutions for instructors.

- Describes step-by-step methodologies to design high-speed circuits as well as layout techniques to maximize both device and circuit performance.
- Contains over 100 end-of-chapter problems and numerous solved examples to aid and test understanding.
- Includes device and circuit simulation and design labs based on real-life scenarios in advanced SiGe BiCMOS and nanoscale CMOS technologies.

**Sorin Voinigescu** is a Professor at the University of Toronto, where his research and teaching interests focus on nanoscale semiconductor devices and their application in integrated circuits at frequencies beyond 300GHz. The co-founder of Quake Technologies, Inc., he was a recipient of the Best Paper Award at the 2001 IEEE Custom Integrated Circuits Conference, 2005 IEEE Compound Semiconductor IC Symposium (CSICS), and of the Beatrice Winner Award at the 2008 IEEE International Solid State Circuits Conference (ISSCC). His students have won Student Paper Awards at the 2004 VLSI Circuits Symposium, the 2006 RFIC Symposium, and at the 2008 and 2012 International Microwave Symposia.

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# High-Frequency Integrated Circuits

## SORIN VOINIGESCU

University of Toronto



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### **ENDORSEMENTS**

"Destined to become a classic reference in high frequency RFICs, Professor Voinigescu's book will certainly become the reference book in the field of high-frequency RFIC design. It contains a comprehensive coverage of a vast array of integrated circuits and systems, including fundamental circuit design techniques, system analysis, packaging techniques, and measurements. It has an exceptional tutorial value, and presents the state of the art in microwave and millimeter-wave systems-on-chip."

#### Gabriel M. Rebeiz, University of California, San Diego

"Sorin Voinigescu has nicely exploited his wide experience in integrated circuits and devices to generate this book. It covers very broadly the field of high-frequency integrated circuits, designed in advanced silicon and III–V technologies. Both experienced designers and newcomers in the field will appreciate this book. I am very interested by the many detailed design recipes and tricks – often with a link to the underlying IC technologies – that are seldom found in related textbooks."

#### Piet Wambacq, University of Brussels and IMEC

"With its rational and omni-comprehensive approach encompassing devices, circuits, systems, and applications, Sorin Voinigescu's book is a unique encyclopedic 'dictionary' for an in-depth understanding of high-speed and high-frequency microelectronic design.

Original, dense of details, clear and focused on the modern design challenges, it removes at the root several design dogmas that have conditioned research and development of high-frequency integrated circuits, resulting in the first book of a new class with a profound look at the road ahead."

#### Domenico Zito, University College Cork

*"High-Frequency Integrated Circuits* is the ideal companion for circuit designers wishing to grasp the challenges of circuit design above RF. Professor Voinigescu takes the reader from system specification down to the transistor, and presents the circuit analysis that underlies every RF circuit designer's intuition."

James Buckwalter, University of California – San Diego

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## CONTENTS

	Preface			
1	Introduction			
	1.1 High-frequency circuits in wireless, fiber-optic, and imaging systems	1		
	1.2 A brief history of high-frequency integrated circuits	2		
	1.3 What does the future hold?	9		
	1.4 The high-frequency IC design engineer	12		
	References	13		
2	High-frequency and high-data-rate communication systems	14		
	2.1 Wireless and fiber-optic communication systems	14		
	2.2 Radio transceivers	15		
	2.3 Modulation techniques	16		
	2.4 Receiver architectures	24		
	2.5 Transmitter architectures	30		
	2.6 Receiver specification	35		
	2.7 Transmitter specification	48		
	2.8 Link budget	50		
	2.9 Phased arrays	52		
	2.10 Examples of other system applications	62		
	Summary	72		
	Problems	72		
	References	75		
3	High-frequency linear noisy network analysis	77		
	3.1 Two-port and multi-port network parameters	77		
	3.2 Noise	91		
	3.3 Two-port and multi-port noise	99		
	3.4 Noise in circuits with negative feedback	117		
	Summary	138		
	Problems			
	References			

Cambridge University Press 978-0-521-87302-4 — High-Frequency Integrated Circuits Sorin Voinigescu Frontmatter <u>More Information</u>

viii	Contents			
4	High-frequency devices	142		
	4.1 High-frequency active devices	142		
	4.2 The nanoscale MOSFET	164		
	4.3 The heterojunction bipolar transistor	219		
	4.4 The high electron mobility transistor	254		
	4.5 High-frequency passive components	274		
	Summary	311		
	Problems	312		
	References	314		
5	Circuit analysis techniques for high-frequency integrated circuits	318		
	5.1 Analog versus high-frequency circuit design	318		
	5.2 Impedance matching	321		
	5.3 Tuned circuit topologies and analysis techniques	335		
	5.4 Techniques to maximize bandwidth	342		
	5.5 Challenges in differential circuits at high frequency	356		
	5.6 Non-linear techniques	362		
	Summary	366		
	Problems	367		
	References	372		
6	Tuned power amplifier design	374		
	What is a tuned power amplifier?	374		
	6.1 Tuned PA fundamentals	375		
	6.2 Classes of tuned PAs and the associated voltage waveforms	377		
	6.3 Linear modulation of PAs	400		
	6.4 Class A PA design methodology	401		
	6.5 Non-idealities in PAs	406		
	6.6 Implementation examples of CMOS and SiGe HBT mm-wave PAs	407		
	6.7 Efficiency enhancement techniques	416		
	6.8 Power combining techniques	425		
	Summary	432		
	Problems	432		
	References	436		
7	Low-noise tuned amplifier design	439		
	7.1 LNA specification and figure of merit	439		
	7.2 Design goals for tuned LNAs	441		
	7.3 Low-noise design philosophy and theory	441		
	7.4 LNAs with inductive degeneration	449		
	7.5 Power-constrained CMOS LNA design	467		

Cambridge University Press 978-0-521-87302-4 — High-Frequency Integrated Circuits Sorin Voinigescu Frontmatter <u>More Information</u>

		Contents	ix
	7.6 Low-current CMOS inverter LNAs		469
	7.7 Low-voltage LNA topologies		471
	7.8 Other LNA topologies		473
	7.9 Differential LNA design methodology		486
	7.10 Process variation in tuned LNAs		486
	7.11 Impact of temperature variation in tuned LNAs		488
	7.12 Low-noise bias networks for LNAs		488
	7.13 MOSFET layout in LNAs		490
	Summary		491
	Problems		491
	References		501
8	Broadband low-noise and transimpedance amplifiers		503
	8.1 Low-noise broadband high-speed digital receivers		503
	8.2 Transimpedance amplifier specification		507
	8.3 Transimpedance amplifier design		510
	8.4 Other broadband low-noise amplifier topologies		535
	8.5 DC offset compensation and VGA-TIA topologies		540
	Summary		545
	Problems		545
	References		551
9	Mixers, switches, modulators, and other control circuits		553
	What is a mixer?		553
	9.1 Mixer fundamentals		553
	9.2 Mixer specification		566
	9.3 Mixer topologies		569
	9.4 Design methodology for downconverters		586
	9.5 Upconverter mixer design methodology		588
	9.6 Examples of mm-wave Gilbert cell mixers		589
	9.7 Image-reject and single-sideband mixer topologies		593
	9.8 Mixer simulation		600
	9.9 Switches, phase shifters, and modulators		600
	9.10 Gilbert cell layout		613
	Problems		615
	References		618
10	Design of voltage-controlled oscillators		621
	What is an oscillator?		621
	10.1 VCO fundamentals		621
	10.2 Low-noise VCO topologies		638

х

Cambridge University Press 978-0-521-87302-4 — High-Frequency Integrated Circuits Sorin Voinigescu Frontmatter <u>More Information</u>

	10.3 VCO simulation techniques	665
	10.4 VCO design methodology	671
	10.5 Frequency scaling and technology porting of CMOS VCOs	675
	10.6 VCO layout	680
	10.7 Mm-wave VCO examples	681
	Summary	686
	Problems	686
	References	696
11	High-speed digital logic	698
	11.1 Systems using high-speed logic	699
	11.2 High-speed digital logic families	705
	11.3 Inductive peaking	721
	11.4 Inductive broadbanding	724
	11.5 Design methodology for maximum data rate	724
	11.6 BiCMOS MOS-HBT logic	725
	11.7 Pseudo-CML logic	729
	11.8 Other bipolar, MOS and BiCMOS CML, and ECL gates	731
	11.9 Dividers	734
	11.10 CML/ECL gate layout techniques	741
	Summary	747
	Problems	748
	References	753
12	High-speed digital output drivers with waveshape control	756
	What is a high-speed digital output driver?	756
	12.1 Types of high-speed drivers	757
	12.2 Driver specification and FoMs	757
	12.3 Driver architecture and building blocks	764
	12.4 Output buffers	765
	12.5 Predriver	781
	12.6 Examples of distributed output drivers operating at 40Gb/s and beyond	787
	12.7 High-speed DACs	795
	Summary	799
	Problems	799
	References	801
13	SoC examples	803
	What is a high-frequency SoC?	803
	13.1 Design methodology for high-frequency SoCs	803

Cambridge University Press 978-0-521-87302-4 — High-Frequency Integrated Circuits Sorin Voinigescu Frontmatter <u>More Information</u>

	Contents	xi
13.2 Transcei	ver architectures, packaging, and self-test for mm-wave radio, radar,	
and imag	ging sensors	812
13.3 60GHz j	bhased array in SiGe BiCMOS versus 65nm CMOS	820
13.4 77GHz	4-channel automotive radar transceiver in SiGe HBT technology	830
13.5 70–80G	Hz active imager in SiGe HBT technology	835
13.6 150-168	GHz active imaging transceiver with on-die antennas in	
SiGe Bi	CMOS technology	843
Summary		846
Problems		846
References		848
Appendix 1	Trigonometric identities	851
Appendix 2	Baseband binary data formats and analysis	852
Appendix 3	Linear matrix transformations	858
Appendix 4	Fourier series	861
Appendix 5	Exact noise analysis for a cascode amplifier with inductive degeneration	862
Appendix 6	Noise analysis of the common-emitter amplifier with transformer	
	feedback	864
Appendix 7	Common-source amplifier with shunt-series transformer feedback	866
Appendix 8	HiCUM level 0 model for a SiGe HBT	868
Appendix 9	Technology parameters	869
Appendix 10	Analytical study of oscillator phase noise	876
Appendix 11	Physical constants	890
Appendix 12	Letter frequency bands	891
Index		892

I

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#### PREFACE

The field of monolithic microwave integrated circuits (MMICs) emerged in the late 1970s and early 1980s with the development of the first GaAs MESFET and pseudomorphic high electron mobility transistor (p-HEMT) IC technologies and started to thrive in the mid-to-late 1990s once the performance of silicon transistors became adequate for radio frequency (RF) applications above 1GHz. Since then, CMOS, SiGe BiCMOS, and III-V HEMT, and heterojunction bipolar transistor (HBT) technology scaling to nanometer dimensions and THz cutoff ( $f_T$ ) and oscillation frequencies ( $f_{MAX}$ ) has continued unabated. Despite the increasing dominance of CMOS, each of these technologies has carved its own niche in the high-speed, RF, microwave, and mm-wave IC universe. Today's nanoscale 3-D tri-gate MOSFET is a marvel of atomiclayer and mechanical strain engineering with more "exotic" materials, heterojunctions, and compounds than any SiGe HBT or III-V device. Indeed, InGaAs and Ge are expected to displace silicon channels in "standard" digital CMOS technology sometime in the next five to ten years. More so than in the past, it is very important that high-frequency circuit designers be familiar with all these high-frequency device technologies.

Apart from the general acceptance of CMOS as a credible RF technology, during the last decade "digital-RF" has radically changed the manner in which high-frequency (HF) circuit design is conducted. Traditional RF building blocks such as low-noise amplifiers (LNAs), voltage-controlled oscillators (VCOs), power amplifiers (PAs), phase shifters, and modulators have greatly benefited from this marriage of digital and microwave techniques and continue to play a significant role well into the upper mm-wave frequencies. New, digital-rich, radio transceiver architectures have emerged based on direct RF modulators and IQ power DACs, fully digital PLLs, and digitally calibrated phased arrays.

Increased device speed makes silicon an attractive technology for emerging mm-wave applications, such as 4Gb/s wireless HDTV links at 60GHz, automotive radar at 77GHz, and active and passive imaging at 94GHz. III-V based and, soon, silicon submillimeter wave sensors with integrated antennas are becoming feasible, and undoubtedly more applications will materialize. A similar scenario is unfolding in wireline and fiber-optic links, where higher-frequency applications such as 110Gb/s Ethernet have recently been standardized by the IEEE.

At the same time, the task of designing high-frequency building blocks becomes increasingly difficult in the nanoscale era. While power dissipation, high-frequency noise figure, and phase noise performance improve with scaling, other critical aspects such as maximum output swing, linearity, and device leakage are all degraded. Lower supply voltages constrain the number of devices which can be vertically stacked. From an economics perspective, the high mask costs of these technologies make first-pass design success a must.

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#### xiv

#### Preface

Nanoscale MOSFETs do not exhibit the classical behavior described in undergraduate textbooks. Foundries frequently supply high-frequency data such as  $f_T$  or minimum noise figure ( $NF_{MIN}$ ), but how can the design engineer incorporate these data into a design? Is "back-of-the-envelope" design still possible in 32nm CMOS at 77GHz? How about 180GHz? Are there optimal solutions for high-frequency IC building blocks? Can they be seamlessly scaled between technology nodes? Such design methodologies are not covered in any textbook, but are fairly well known – in some circles – to produce robust RF, mm-wave, and wireline IC designs that are generally transferable between technology nodes and even between III-V and silicon technologies. In the nanoscale era, the link between circuit and device performance grows in importance, and successful designers must be well versed in both areas.

This book grew out of a set of notes, assignments, and projects developed and taught during the last nine years as an advanced graduate course at the University of Toronto. Although starting from the basic concepts, the material delves deep into advanced IC design methodologies and describes practical design techniques that are not immediately apparent and which are rooted in over 20 years of microwave and mm-wave silicon and III-V IC design experience. It provides a design intensive overview of high-speed and high-frequency monolithic integrated circuits for wireless and broadband systems with an emphasis on device-circuit topology interaction and optimization. The central design philosophy is that "the circuit is the transistor," and that maximizing transistor and circuit performance go hand-in-hand. The textbook features an extensive treatment of high-frequency semiconductor devices and IC process engineering fundamentals. Properties of CMOS FETs and SiGe HBTs are examined in the context of maximizing transistor performance for high-speed, low-noise, large power, and/or highly linear circuits. Alternative device structures, such as SOI and multi-gate 3-D channels, are presented to keep the reader up-to-date with the latest technology trends. Additionally, compound semiconductor technologies (InP, GaAs, GaAsSb, and GaN), are covered. This topic, which is largely ignored in previous textbooks, is beneficial to a number of practicing engineers as these technologies continue to be incorporated in a number of wireless and wireline production parts today. Furthermore, channel strain engineering, SiGe source-drain heterojunctions, and stacked gate dielectrics speak of the many similarities between state-of-the-art CMOS and III-V heterojunction FETs.

Circuit layout often can make the difference between a successful or unsuccessful high-speed design. For the first time in a textbook in this area, layout techniques that maximize both device and circuit performance are included.

Based on the underlying device fundamentals, step-by-step design methodologies for wireless and wireline building blocks are presented. Circuit design is taught from a current-density centric biasing approach, which relies on biasing transistors at or near their peak  $f_T$ , peak  $f_{MAX}$ , or optimal  $NF_{MIN}$ . Despite the complexity of modern transistors, it is shown through examples that simple design equations and hand analysis are critical and often sufficient for successful designs even at mm-wave frequencies. Numerous practical design examples, validated by fabrication and measurements, are included for bipolar and FET circuits implemented in bulk and SOI CMOS, SiGe BiCMOS, InP, GaAs, and GaN technologies.

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Preface

Differential, single-ended, and half-circuit noise and impedance matching, stability issues and common misconceptions about differential signaling, noise in feedback circuits, and velocity saturation in nanoscale CMOS are addressed for the first time in this textbook.

RF CMOS designers often complain about model inaccuracies. This book for the first time shows that, through knowledge of CMOS technology scaling rules, engineers can design CMOS high-speed circuits that are robust to bias current and threshold voltage variations, even in the absence of transistor models. Moreover, this understanding of technology scaling allows for designs to be ported between technology nodes, with little-to-no redesign required.

Gate finger segmentation of MOSFETs and Gilbert cells is described as a general technique of providing multi-bit digital control and calibration of high-frequency attenuators, switches, amplifiers, and phase shifters along with on-chip at speed self-test methodologies.

High-frequency IC design is as much an art as it is a science. The art comes from knowing when, what, and how to approximate and simplify, what aspect of a transistor model, simulation or measurement can be trusted and when. It is best acquired by working with experienced designers, learning from their mistakes, and by spending many hours conducting hands-on experiments in the lab. To support the latter aspect, several practical assignments and projects on RF, mm-wave, and optical fiber circuits using nanoscale RF CMOS, SiGe BiCMOS, and III-V technologies are provided as supplementary material on the website.

The book has 13 chapters which are organized in two large sections: (i) foundations of HF IC design, consisting of Chapters 2 through 5, and (ii) HF building block design methodologies, covered in Chapters 6 through 12. Additionally, Chapter 13 surveys representative examples of recent mm-wave silicon systems on chip, SoCs.

Chapter 1 gives a brief history of the field of high-frequency integrated circuits and can be assigned for home reading.

Chapter 2 provides an overview of wireless, fiber-optic, and high-data-rate wireline systems, transceiver architectures, and modulation techniques and explains how they impact the specification of high-frequency ICs.

Chapter 3 briefly reviews multi-port network parameters, *S*-parameters, and the Smith Chart, and introduces the key concepts of noise temperature, noise figure, correlated noise sources, noise parameters, and optimal noise impedance. Analysis techniques for high-frequency linear noisy networks, noise matching bandwidth, optimal noise impedance matching in multi-ports, negative feedback, and differential circuits are treated in depth.

Chapter 4, the largest, consists of five sections, and requires two-three lectures, each two hours long, for complete coverage. It focuses on the small signal, noise, and large signal characteristics, modeling, optimal biasing, sizing and layout of high-frequency field-effect, and heterojunction bipolar transistors fabricated in silicon and III-V technologies. The first section discusses the common high-frequency and noise characteristics of FETs and HBTs, as needed for HF circuit design, and explains the impact of noise correlation and the physical reasons why the noise and input impedances of transistors are different. The last section of Chapter 4 addresses the design and modeling of silicon integrated inductors, transformers, varactor diodes, capacitors, resistors, as well as interconnect modeling. If students have a solid background in advanced semiconductor devices, only Sections 1 and 5 need to be covered. I usually

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#### Preface

xvi

teach Sections 4.2, 4.3, and 4.4 as part of a separate undergraduate/graduate course on advanced electronic devices. These sections discuss the physics, high-frequency, and noise equivalent circuit and layout of nanoscale MOSFETs, HBTs, and HEMTs, respectively, at a fairly detailed and advanced level.

Chapter 5 completes the first half of the textbook with a survey of high-frequency tuned and broadband circuit topologies, impedance matching, bandwidth extension, and circuit analysis techniques. It includes an extensive treatment of stability, common-mode rejection, and single-ended to differential-mode conversion in high-frequency differential circuits. The chapter ends with a description of general topologies and hand analysis methodologies for non-linear circuits, with differential doublers and triplers as main examples.

Chapter 6 introduces another fundamental HF IC concept foreign to both analog and digital circuit designers: that of large signal impedance, which forms the basis of optimal output power matching of transistors in power amplifiers. This chapter deals with the basic principle of operation, classes, topologies, analysis, and step-by-step design methodologies for tuned power amplifiers. Solved PA design problems are provided in CMOS, GaN, and SiGe HBT technologies along with efficiency enhancement and power-combining techniques.

Building up on the optimal noise impedance concept of Chapter 3 and the optimal transistor biasing and sizing techniques developed in Chapter 4, Chapter 7 discusses the specification, design philosophy, topologies, and algorithmic design methodologies for tuned low-noise amplifiers, along with the theory and examples of LNA frequency scaling and design porting from one CMOS technology node to another.

Chapter 8 follows up on the low-noise theme with the design theory and analysis of broadband low-noise transimpedance and transimpedance-limiting amplifiers with digital gain control for fiber-optic and wireline applications.

Chapter 9 examines a variety of non-linear control circuits, largely based on switches, hybrid couplers, and phase shifters, and ranging from mixers to tuned variable gain amplifiers, direct modulators, and tuned high-frequency digital-to-analog converters. The basic concepts of frequency conversion, image frequency, image rejection, analog and digital phase shifting are introduced along with non-linear signal and noise analysis methodologies and simulation techniques. Step-by-step design methodologies for upconvert and downconvert mixers, digital attenuators, and tuned RF DACs and modulators are described along with circuit examples at frequencies as high as 165GHz.

Chapter 10 rounds up the review of non-linear and low-noise circuits with an in-depth treatment of voltage-controlled oscillators. Specification, topologies, analysis, and simulation techniques, and step-by-step design methodologies focusing on minimizing phase noise or power consumption are discussed in detail. For those interested in a deeper understanding of the physical origins of phase noise, the companion Appendix 10 presents an analytical harmonic series formalism to explain how partially correlated noise sidebands, caused by noise sources internal to the oscillator, arise around the carrier in the frequency spectrum of an oscillator.

Chapters 11 and 12 focus on the design of high-speed logic gates and large swing, broadband output drivers, respectively. Algorithmic design methodologies are developed for current-mode logic (CML) FET, HBT, and FET-HBT families with design examples in silicon and III-V

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Preface

xvii

technologies. Static, dynamic, and injection-locked divider stages based on CML gates are covered in Chapter 11. The design of laser drivers, optical modulator drivers, and of large swing, broadband power DACs for 40 and 110Gb/s fiber-optic networks with QAM and OFDM modulation formats are discussed in Chapter 12.

Chapter 13 ties it all together with a comprehensive description of a HF design flow, system integration, isolation, simulation, and verification strategies for HF silicon SoCs. Examples of commercial single-chip 60GHz and 77GHz phased array transceivers for short-range, gigabit data-rate wireless communication, automotive radar, and active imaging are discussed in detail, along with a 150GHz SiGe BiCMOS single-chip transceiver with PLL, two receive channels, and integrated transmit and receive antennas.

Although the book is self-contained and each topic is introduced from first principles, it is expected that the reader has an undergraduate level background in semiconductor devices, analog circuits, and microwave circuits.

Chapters 2 through 12 can be taught in twelve two to three hour long lectures. Chapters 6 through 12 can be covered in any order as long as Chapters 8 and 9 are taught after Chapter 7 and Chapter 12 follows Chapter 11. Alternatively, to expose the students to circuit design earlier in the course, the second half of Chapter 3 (noise in circuits with negative feedback) and Section 5 of Chapter 4 can be taught after Chapters 5 and 6. In an RF-only course, Chapters 8, 12 (and even 11) can be left out.

This book was written over the course of six years during which some sections have been updated to keep up with the frantic pace of change in this still fast-evolving field. Despite many efforts to correct mistakes and avoid repetition, errors likely still remain. I shall be thankful to fix them as soon as I receive feedback from readers.

Many people have contributed to this book directly and many more indirectly or unbeknownst to me. I apologize to the latter. Chapter 2 benefited from many discussions on 60GHz wireless system specifications with Nir Sasson and Dr. Magnus Wiklund. The groundwork for the theory of noise in circuits with negative feedback in Chapter 3 were laid out in the late 1980s while collaborating with Dan Neculoiu on developing a low-noise amplifier design project course at the Electronics Department of the Politehnica University in Bucharest. The section on FinFETs and high-frequency parasitics of MOSFETs in Chapter 4 benefited from the discussions with Dr. Ian Young of Intel and Dr. Jack Pekarik of IBM. I am also particularly grateful to Dr. Timothy (Tod) Dickson of IBM for kickstarting Chapters 7, 8, and 11 and for many figures from his Ph.D. thesis. Professor Emeritus Miles Copeland of Carleton University wrote Appendix 10 and painstakingly reviewed Chapter 10, providing many valuable suggestions over lengthy and frequent phone calls. I would like to thank Dr. Pascal Chevalier of STMicroelectronics, Crolles, France, for numerous discussions on SiGe HBTs, SiGe BiCMOS, and nanoscale CMOS physics and process flows. Chapter 13 was enhanced through the gracious help of Dr. Herbert Knapp and Dr. Marc Tiebout of Infineon, and of Dr. Juergen Hasch of Robert Bosch GmbH. who have provided advanced copies of the graphical material used for the description of the 77GHz automotive radar and imaging chip-sets, and who have carefully reviewed the associated text in Chapter 13. Dr. Juergen Hasch also contributed, along with former

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#### xviii Preface

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