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Advanced Model Order Reduction Techniques in VLSI Design

Model order reduction (MOR) techniques are important in reducing the complexity of nanometer VLSI designs, and consequently controlling "parasitic" electromagnetic effects, so that higher operating speeds and smaller feature sizes can be achieved. This book presents a systematic introduction to, and treatment of, the key MOR methods used in general linear circuits, using real-world examples to illustrate the advantages and disadvantages of each algorithm.

Starting with a review of traditional projection-based techniques and proofs of some fundamental theories, coverage progresses to advanced "state-of-the-art" MOR methods for VLSI design. These include HMOR, passive truncated balanced realization (TBR) methods, efficient inductance modeling via the VPEC model, general model optimization and passivity enforcement methods, passive model realization techniques, and structure-preserving MOR techniques. Numerical methods have been used throughout and, where possible, approached from the CAD engineer's perspective. This avoids complex mathematics, and allows the reader to take on real design problems and develop more effective tools.

With practical examples and over 100 illustrations, this book is suitable for researchers and graduate students of electrical and computer engineering, as well as for practitioners working in the VLSI design and design automation industries.

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Foreword

Interconnect model reduction has emerged as one crucial operation for circuit analysis in the last decade as a result of the phenomenon of interconnect dominance of advanced VLSI technologies. Because interconnect contributes to a significant portion of the system performance, we have to take into account the coupling effects between subcircuit modules. However, the extraction of the coupling renders many small fragments of parasitics. While the values of the parasitics are small, the number of fragments is huge and this makes the accumulated effect non-negligible. If left untreated, the amount of parasitics can gobble up the memory capacity and consume long CPU time during circuit analysis.

Model reduction transforms a system into a circuit of much smaller size to approximate the behavior of the original description. Many researchers have contributed to the advancement of the techniques and demonstrated drastic reduction of the circuit sizes with satisfactory output responses in published reports. Many of these techniques have also been implemented in software tools for applications. However, it is important for the users to understand the techniques in order to use the package properly. To adopt these approaches, we need to inspect the following features.

1. Efficiency of the reduction: the complexity of the reduction algorithm determines the CPU time of the model reduction. The size of the reduced circuit affects the simulation time.
2. Reduction of both model order and terminals of circuits: reduction of terminals was investigated less in the past and combined terminal and model order reduction leads to more compact models.
3. Robustness of the algorithms: the numerical stability of the reduction algorithm ensures the robustness of the operation.
4. Structure of the reduced systems: the reduced systems may or may not preserve important characteristics like symmetry, reciprocity, etc. Those structure characteristics are important for reduction itself and for systems using the models.
5. Realizablility of the reduced system: the reduced system is realizable if it is passive and we can implement it using electrical elements with positive or negative values. We can simulate a realizable system with general simulation tools. Otherwise, we need to check if the reduced system satisfies the constraints of the simulation package.
6. Passivity of the reduced circuits: the passivity ensures that the simulation

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outputs are bounded for bounded inputs even if the reduced circuit is combined with other passive subcircuits.

7. Error bounds: The error bounds of the output responses provide users with confidence in the results.

In this book, Professors Sheldon X.-D. Tan and Lei He presented a comprehensive description of the reduction techniques. They have provided motivations for the approaches and insights into the algorithms as active researchers in the field. I found that the treatment of the subject is innovative and the general description is pleasant to read. The book covers the contemporary results and opens windows on future research directions in the field.

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Some of the materials in this book come from the graduate level course notes of EE213, Computer-aided electronic circuit simulation, taught by Sheldon Tan at UC Riverside, who would like to thank his students in this course for developing those notes in the past three years.

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