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0521022347 - Sub-Half-Micron Lithography for ULSIs
Edited by Katsumi Suzuki, Shinji Matsui and Yukinori Ochiai
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Introduction 1

Masao Fukuma

The first commercial 0.25-μm technology was distributed to users in 1997, and is now widely used in advanced ULSIs (e.g. 64-Mb and 256-Mb DRAMs, high-end microprocessors, and ASICs). 0.18-μm technology has been developed for commercial release in 1999, and 0.13-μm technology is in the research phase.

Because lithography is a key process in the fabrication of high-performance ULSIs, this book reviews ULSI technology trends and discusses lithography requirements. It then describes in detail the most widely used optical lithography technologies as well as representative next-generation lithography technologies such as X-ray lithography, electron-beam lithography, and ion-beam lithography.

1.1 Device technology trends

1.1.1 Logic devices

Because high speed is a first priority for logic ULSIs, there have been many efforts to increase MOSFET driving capability and reduce parasitic effects. Figure 1.1 shows the technology 'roadmap' for logic-oriented CMOS devices. The driving capability is increased by making the gate oxide as thin as possible and using a carefully designed impurity profile. Gate, source, and drain resistances are reduced by using a salicide process. An n–n gate structure (n^+ gates for both n- and pMOSFETs) has been chosen for design rules down to 0.35 μm, but a p–n gate structure (n^+ for nMOSFETs and p^+ for pMOSFETs) is used when the design rule is less than 0.25 μm because the p^+ gate provides a surface channel in the pMOSFET and this results in smaller short-channel effects and a higher driving capability at a lower threshold voltage.

Experimental 0.04-μm nMOSFET[1†] and 0.07-μm CMOS devices[2] have been reported, and Figure 1.2 shows a SEM cross-section of, and waveform for, a 0.07-μm CMOS ring oscillator with a delay time of 14 ps. This dynamic performance is excellent, but the oxide thickness of the MOSFETs is about 3.5 nm, which is almost the limit for suppression of the tunneling current. Further downscaling will require the development of a gate insulator with a high dielectric constant or of a circuit that tolerates a small gate leakage current. Simulations suggest that 0.01- to 0.02-μm MOSFETs will show reasonable I–V characteristics and that the CMOS gate delay time will be only a few picoseconds.[3]

On the other hand, wiring delay in a chip is becoming a serious factor limiting ULSI performance. Not only does reducing the width and height of wiring increase the wiring resistance per unit length, but average wiring length in ULSIs also becomes longer as the chip size increases. Furthermore, wiring capacitance is not easily scaled down because fringing and/or coupling capacitance with neighboring wires becomes dominant in fine wiring. As a result, the speed of downscaled ULSI logic devices is limited by wiring delay rather than by intrinsic gate delay. Overcoming this problem will require new materials both for wiring and for interlayer dielectrics. Attention is focusing on

† Numbered references to be found at the end of each chapter.

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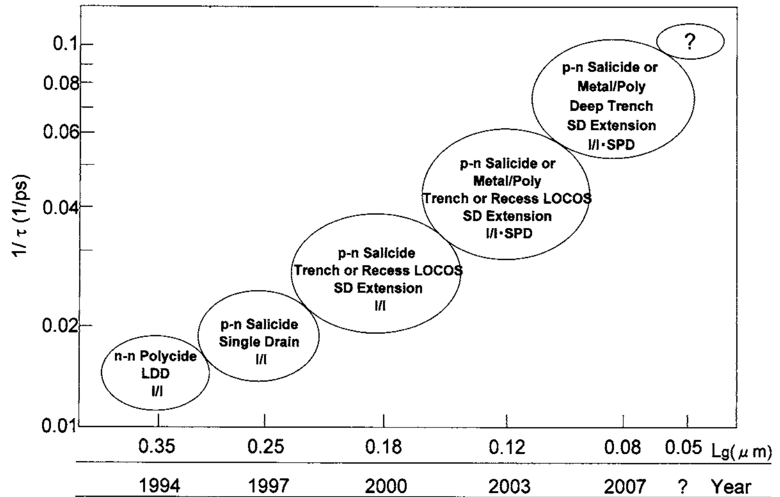
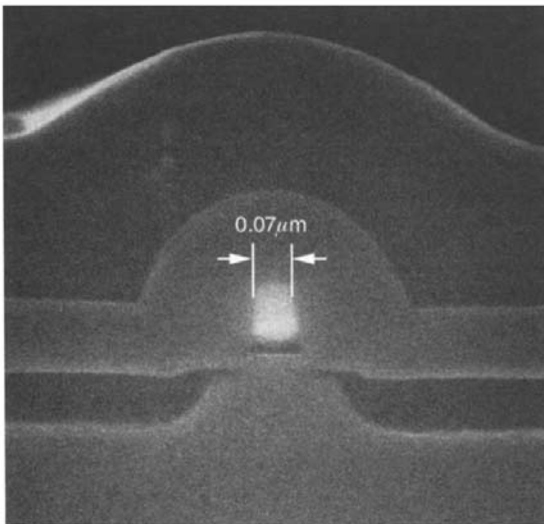
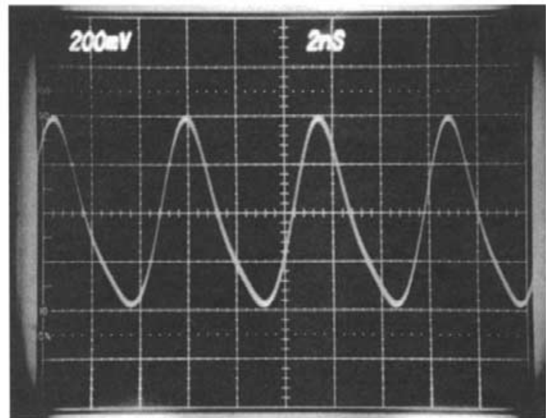


Figure 1.1 Technology 'roadmap' for CMOS devices. τ: propagation-delay time; L_g: width of gate electrode; I/I: ion implantation.



(a)



(b)

Figure 1.2 (a) SEM photograph of cross-section of 0.07-μm-gate-length FET. (b) Waveform of a 201-stage CMOS ring-oscillator. Each division equals 2 ns on x-axis and 200 mV on y-axis.

copper as a low-resistance wiring material, and both SiOF and organic materials seem to be useful as interlayer insulator materials with low dielectric constants. The introduction of these materials will improve LSI performance by about 30%. This improvement, however, will not be great enough to bring us into the 0.1-μm era. Instead, circuit-oriented and architecture-oriented approaches are necessary. Figure 1.3 shows, as a typical example, a scaling

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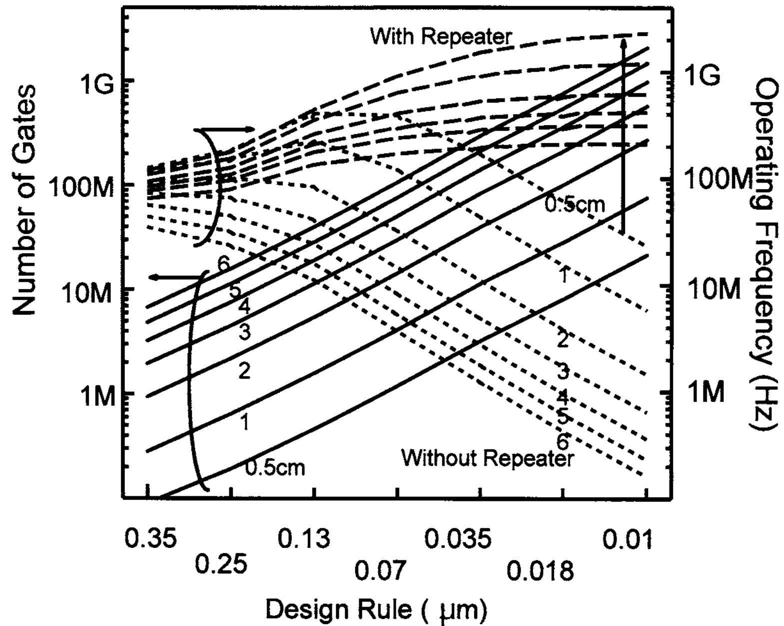

Figure 1.3 Scaling scenario for wiring. Utilizing repeaters and minimizing the size of the functional block which requires high clock frequency are essential requirements.

scenario for wiring with repeaters. Utilizing repeaters and minimizing the size of the functional block that requires a high clock frequency is expected to achieve further performance improvement even when the design rule is less than 0.1 μm.

Mobile applications require circuits that consume little power, and this leads to operating voltages below those expected from the scaling scenario or the conventional scaling 'roadmap'. A 0.9-V supply voltage, for example, is necessary even for the 0.35-μm 'generation'. High performance at such low supply voltages will require breakthroughs both in circuit design and in fabrication technology. Figure 1.4 shows an experimental low-power DSP (digital signal processor) core[4] that uses two types of MOSFET with different threshold voltages and that takes advantage of specially designed stacked CMOS circuits and busses with small signal swing. As a result, its operating frequency is as high as 100 MHz and its power dissipation at 0.9 V is only 4 mW.

In the gigahertz era, power dissipation is becoming more serious not only for mobile applications but also for general applications such as desktop PCs. Research and development on low-power architecture and circuits for low-voltage operation have recently been emphasized as much as the device scaling, and this trend will be seen even in high-end applications.

1.1.2 Memory devices

The DRAM is a typical memory LSI and has been a technology driver in Japan. Today, the capacity of the most advanced commercial DRAM is 256 Mb and that of the most advanced prototype is 4 Gb.

Table 1.1 shows a typical technology trend in DRAMs. To get a sufficient signal on a bit line, modern DRAMs require a cell charge of at least 20 fC, a value that is almost independent of the DRAM 'generation'. This requirement is a big barrier to the development of gigabit

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Table 1.1 *Technology 'roadmap' for DRAMs.*

	1 Mb	4 Mb	16 Mb	64 Mb	256 Mb	1 Gb	4 Gb
Design rule (μm)	1.2	0.8	0.6	0.4	0.25	0.18	0.12
Supply voltage (V)	5		5(3.3)	3.3	3.3(2.5)	3.3(2.0)	2.0(1.5)
DRAM cell structure	{Planar or Stacked or Trench	{Stacked or Trench	Stacked	Stacked with HSG	HSG ring		
Gate electrode	Polycide ⟶						Metal
Drain structure	DDD	LDD ⟶			Single drain		
Isolation	LOCOS	Modified LOCOS ⟶			Trench		
Gate oxide thickness (Å)	200	180	140	110	80	65	50
Capacitor insulator	SiN					Ta_2O_5/BST/STO	
Capacitor insulator thickness (Å)		120	60	50	45	30	
Wiring metal	Al–Si–Cu	Al–Cu				Al(Cu)	Cu
Lithography	g-line		i-line		KrF	KrF + Ps	ArF/X-ray/EB
Etching	RIE		ECR/Magnetron		High-density plasma		

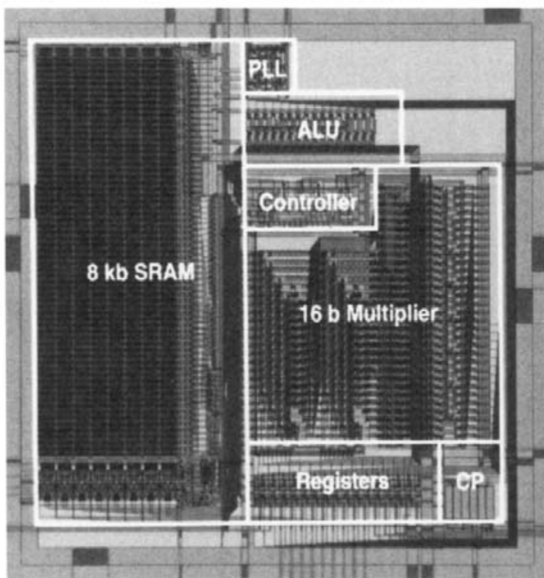

Figure 1.4 100-MHz DSP core based on 0.25-μm CMOS technology. Operating voltage is 0.9 V, and power dissipation is only 4 mW which is 1/50 that of conventional DSPs. Chip size is 1.4×1.4 mm^2.

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DRAMs because the thickness of the cell capacitor dielectric has already reached the physical limit determined by tunneling phenomena. The memory cell in 1-Mb and smaller DRAM has a planar structure, but many types of three-dimensional structures that provide a high capacitance in a smaller structure have been proposed for 4-Mb and larger DRAMs (Figure 1.5). Many DRAM makers are now choosing the stacked trench cell because it can be fabricated more easily than a trench cell.

When the design rule becomes 0.18 μm, however, as it does for DRAMs with capacities between 256 Mb and 1 Gb, the stacked trench cell required cannot be fabricated because it is too tall or its aspect ratio is too large. Two approaches to getting sufficient cell capacitance are to increase the effective area of the capacitor cell and to use a material with a high dielectric constant ϵ. One way to increase the effective area is by making a capacitor electrode with micro-roughness. Figure 1.6 shows a typical example in which hemispherical grain (HSG) polysilicon is used as an electrode.[5] This structure provides twice the capacitor area of a flat capacitor electrode and is reasonably easy to fabricate but is not particularly suitable for further increases in the capacitor area.

The potentially more useful approach is thus to use a material with a higher dielectric constant. Some candidate materials are Ta_2O_5, BST ($Ba_{1-x}Sr_xTiO_3$), and PZT $(Pb, Zr)TiO_3)$, which have dielectric constants ranging from 20 to 5000. Figure 1.7 shows an experimental 4-Gb DRAM[6] using a BST film whose capacitance is equivalent to that of a 0.35-nm-thick S iO_2 layer. This BST film is thin enough that we can use a multi-valued architecture. That is, 2-bit data (four values) can be stored in each cell, resulting in a 4-Gb DRAM with 2-Gb memory cells.

Recently, there have been strong demands for nonvolatile memories that can be used in mobile applications. Static random access memories (SRAMs) work as quasi-nonvolatile memories, but it is difficult to get a high storage capacity with them because their memory cells are large. Because SRAMs operate at high

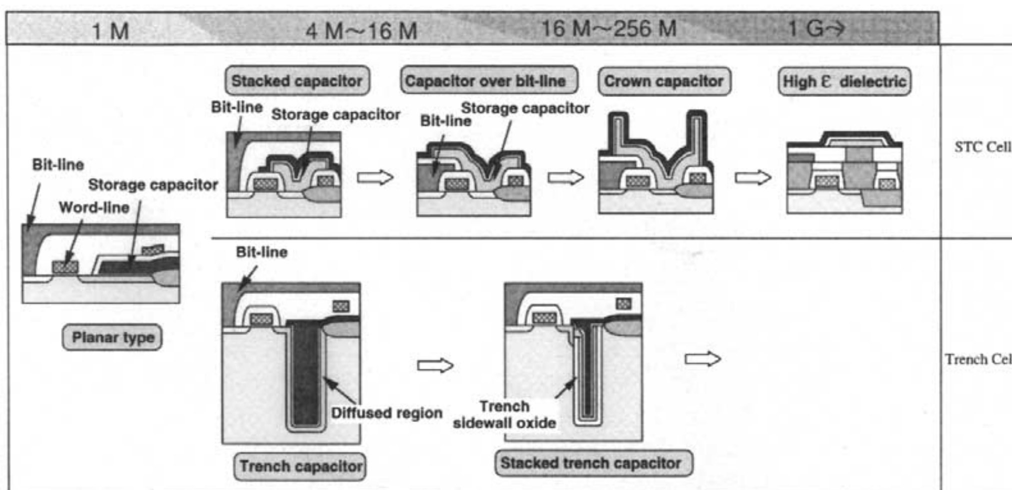

Figure 1.5 Evolution of DRAM cell structure. DRAM capacity is given in bits.

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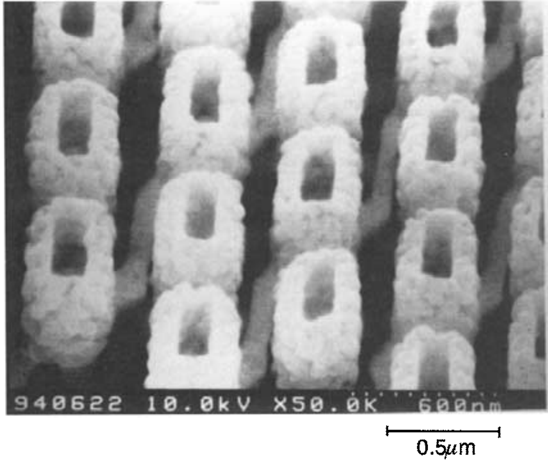

Figure 1.6 HSG capacitor cell used in 1-Gb DRAM.

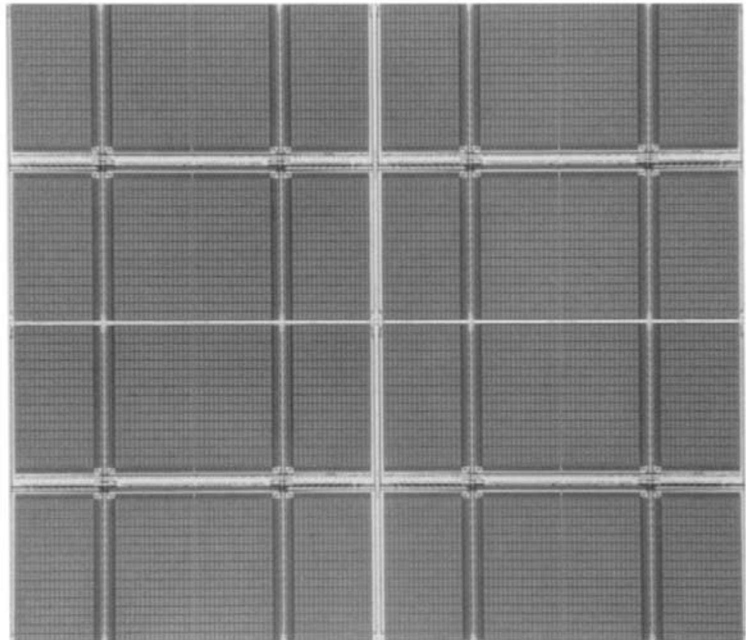

Figure 1.7 Four-level storage 4-Gb DRAM where BST is utilized as cell capacitor insulator. Chip size is 33.9×29.0 mm^2.

speed, they are often used for cache memory. And, because they are easily integrated with logic circuits, they are also often used for on-chip memory. On the other hand, EEPROM and flash memory are also nonvolatile and are going to be widely used in mobile equipment such as digital cameras and IC cards. These nonvolatile memories, however, require more time (ms) for data writing and their applications are limited to ROM-like operations. Markets demand low-cost and high-density nonvolatile RAMs that operate fast. For this reason, FeRAM (ferroelectric RAM) which utilizes a ferroelectric material such as PZT (lead zirconium titanate) and SBT ($SrBi_xTi_yO_z$), is attracting attention. The ideal FeRAM cell, which

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consists of one transistor and one ferroelectric capacitor, would have an access time less than 100 ns and a retention time of 10 years, and would be able to be used as the nonvolatile main memory in mobile computing systems. Figure 1.8 shows an experimental 1-Mb FeRAM[7] in which SBT is used. Although the ferroelectric materials, like the high-dielectric-constant materials for DRAMs, are not easy to bring into the LSI fabrication process used in commercial manufacturing, their introduction would be a real breakthrough to the gigabit era.

We can already integrate more than 10 million transistors even in logic LSIs, and this naturally leads to the SoC 'System on a Chip.' The integration of DRAM and logic devices is advantageous in increasing memory bandwidth while reducing power consumption and assembly costs. Figure 1.9 shows a typical example of DRAM–logic integration, Compress DRAM,[8] in which a 16-Mb DRAM and a graphics data compressor/decompressor are integrated. The bandwidth is 3.2 Gb/s and the power consumption is only 1.4 W.

1.2 Demands for lithography

Lithography was not a limiting factor in scaling the design rule down to 0.35 μm, but it is now becoming a practical limiting factor. Table 1.2 lists typical lithography requirements for DRAM fabrication. There are many factors which should meet specifications for a deep-submicron design rule: resolution, depth of focus (DOF), critical dimension (CD) control, overlay accuracy, field size, throughput, and cost. Among them, CD control and overlay accuracy are the key factors for modern ULSIs. Today's most advanced processors contain more than 10 million transistors. This means that not only pure memory LSIs but also logic LSIs are now going into the six sigma (6σ) era, which requires strict control of

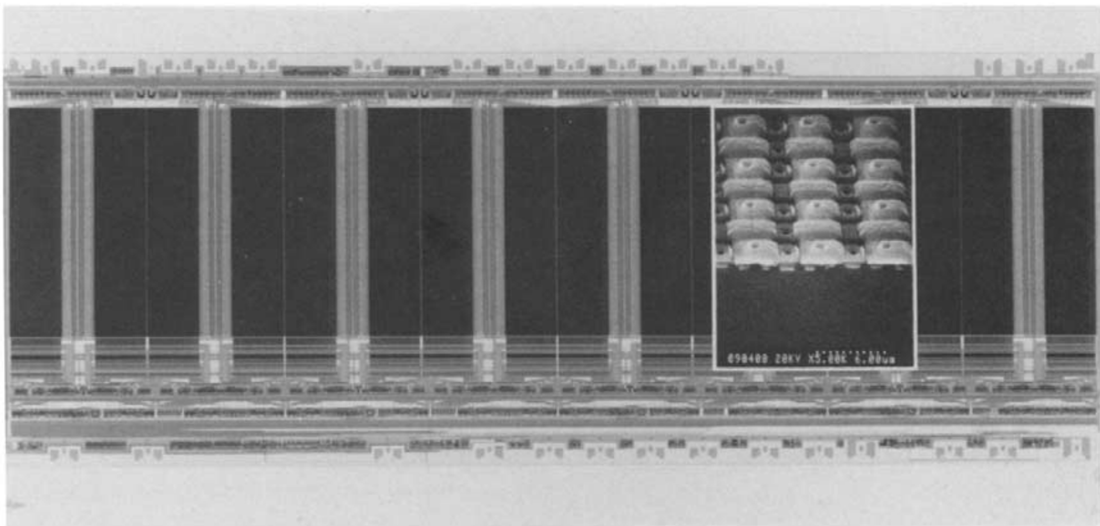

Figure 1.8 60-ns 1-Mb FeRAM. Chip size is 15.7×5.8 mm^2. Inset is a SEM photograph of the FeRAM cells.

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Table 1.2 *Characteristics needed in lithography for DRAM fabrication.*

		64 Mb	256 Mb	1 Gb
Resolution (μm)	Line-and-space	0.35	0.25	0.18
	Window	0.4	0.3	0.2
Depth of focus (DOF) (μm)		1.5	1.2	1.0
Field size (mm^2) (2-chip exposure)		22 × 22 (31.1 mm ϕ)	25 × 25 (35.3 mm ϕ)	33 × 16 (1-chip exposure)
Critical dimension (CD) control (nm) (3σ)		35	25	18
Overlay accuracy (nm) ($\bar{x} + 3\sigma$)		90	60	45

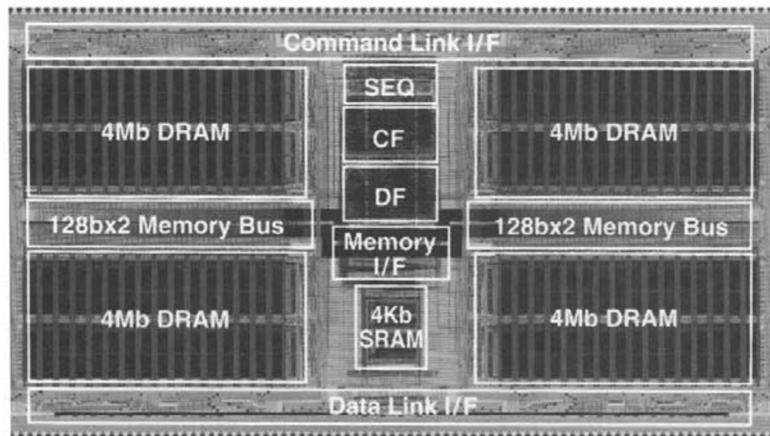

Figure 1.9 Compress DRAM; bandwidth 3.2 Gb/s, power consumption 1.4 W. Chip size is 16.5 × 8.3 mm^2.

device parameters. For example, even if the circuit allows 20% fluctuation in channel length, the standard deviation in the channel length should be less than 4–5 nm when the design rule is 0.13 μm. Beam uniformity and stable resist processes are key factors for reducing line-width fluctuation. For logic applications, pattern-size adjustment is also necessary because of the pattern irregularity of logic devices.

Overlay accuracy is a serious concern in the fabrication of high-density memories. Figure 1.10 shows, for various design rules, the calculated relationship between DRAM cell size and overlay margin. In the high-density memory, the overlay accuracy has an impact on memory size similar to that of the resolution.

Depth of focus is another key factor, especially in the case of optical lithography. The surface profile of ULSI devices depends on the type of circuit and the type of device structure. The critical topographical steps in the recent DRAM cell are: the step at the isolation boundary, the step at the gate structure, and the step at the capacitor. The last one is the most critical. To achieve the required resolution in practical

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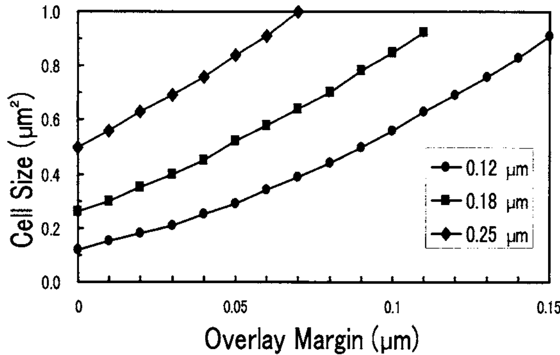

Figure 1.10 Relationship between DRAM cell size and overlay accuracy where design rule is a parameter.

device-fabrication processes, planarization is usually employed. Such a process, however, increases chip-fabrication cost.

Although many research and development activities have been devoted to lithography for device rules smaller than 0.1 μm, there is still no lithography technology suitable for devices whose design rule is less than 0.1 μm. The key factors are still resolution, CD control, overlay accuracy, field size, depth of focus, and throughput. As discussed in Section 1.1, 0.07-μm CMOS devices have been demonstrated experimentally, and simulations have predicted that it will be possible to make high-performance MOS ULSIs with a channel length of 0.01 μm. The fundamental scaling limit is thus far from the scale of present MOS devices. Practical lithography for sub-tenth-micron devices will therefore be one of the most important themes for the next 5 years.

1.3 Conclusion

Multimedia systems need high-speed, low-power and high-density ULSI devices in which sub-tenth-micron technology will be utilized. Both experimental and theoretical analyses predict that such devices could be developed within 10 years. Many problems related to fabrication processes, device structures, circuit configurations, system architectures and design methodology need to be solved, and one of the most serious is lithography. Developing practical lithography technology for Si ULSIs having design rules of 0.1 μm or less is essential if we are to establish a real multimedia society in the world of the 21st century.

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Optical lithography 2

Kunihiko Kasama, Shinji Okazaki, Hisatake Sano
and Wataru Wakamiya

2.1 Introduction

Optical lithography has been widely used for fabricating semiconductor devices for more than 30 years. The principle of optical lithography is the same as that of photography: wafers are coated with a photosensitive material (resist) and patterns are exposed on the resist using optical tools.

The trends in the minimum feature size of memory devices and the major optical lithographic tools used for patterning are shown in Figure 2.1. Several types of optical tools have been used in the fabrication of semiconductor devices, and resolution has been improved by changing the exposure systems and exposure wavelengths (Figure 2.2).

In this chapter, we will describe optical lithography technology. After outlining the history and principles of optical lithography, recent representative optical lithography technologies, such as i-line- and DUV-lithography, are

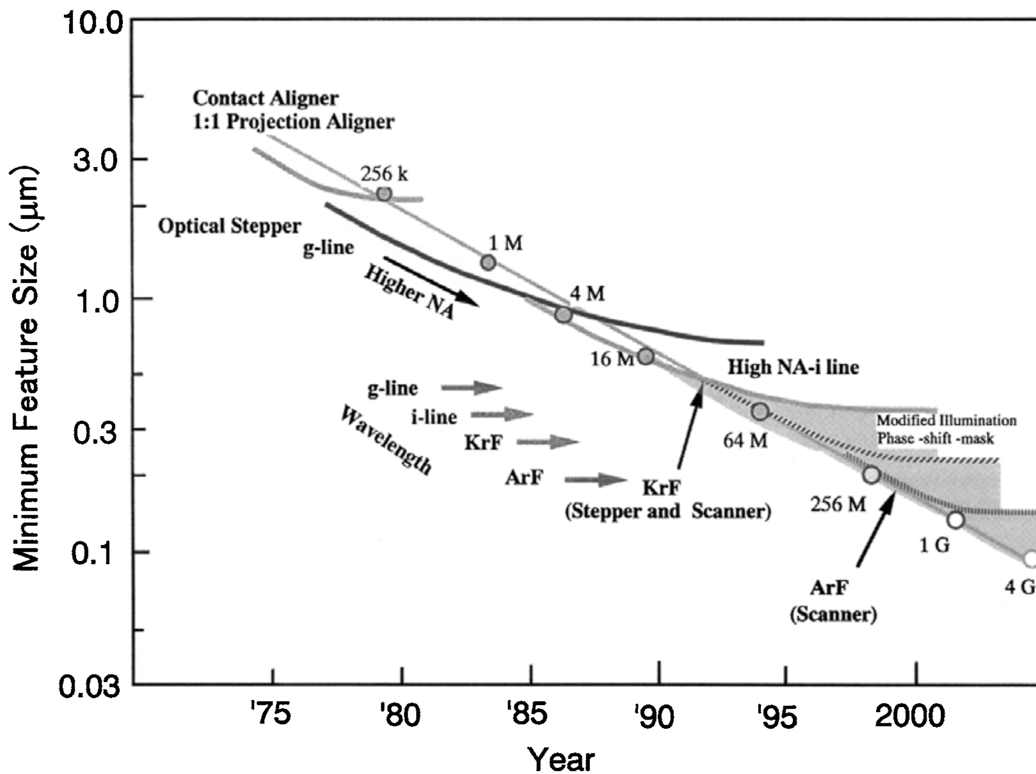

Figure 2.1 Miniaturization trends of DRAM pattern size and development of optical lithographic tools. DRAM capacity is given in bits.

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