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Carbon-based Materials as Key-enabler for "More Than Moore"

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ABSTRACT

Carbon-based materials like nanotubes and graphene are heavily investigated as future transistor devices and in interconnect applications. While much of the interest has been devoted to the device aspects in competition to conventional transistors, the paper here will focus on some less known applications of pyrolytically deposited carbon. Proposed and demonstrated are applications in capacitors, gate materials, through-silicon vias, novel non-volatile memories, carbon-silicon Schottky diodes and sensors.

INTRODUCTION

Common scaling in microelectronics relied on Moore's Law, which holds that the number of transistors on a chip doubles every 18 months. Having more transistors on a given chip area means more speed, more functions and cheaper products. However, in many cases, these integrated circuits make up only a small percentage of a complete system, like a cell phone, where other components need to be integrated to create multi-function devices. The “More than Moore” approach, as described by the International Technology Roadmap for Semiconductors (ITRS) predicts further growth prospects for system integration, if bulky discrete active and passive components—such as memories, processors, resistors, capacitors, diodes and sensors - can be assembled and integrated to form more efficient systems. This paper describes industrial efforts to use the high electric conductivity and conformal deposition property of pyrolytic carbon in many different “More than Moore” applications.

Carbon nanotubes and graphene have been investigated for application in microelectronics over the past few years. For application as interconnects, nanotubes and graphene have been pursued intensively, due to their low specific resistivity. However, for real interconnect applications, many nanotubes and graphene layers need to be bundled for parallel operation in order to make their overall resistance comparable or even better than conventional metallization schemes [1]. Stacking graphene leads simply to the formation of graphite, whereby the specific resistivity of the stacked graphene layers gets worse again and approaches the value of graphite. However, graphite’s in-plane resistivity can be as low as 50 μΩcm and can be engineered down to 1 μΩcm by doping and intercalation. Only recently, de Heer’s group was able to grow graphene stacks, which showed no deterioration as the layer thickness increased, but it required a special SiC substrate and very high temperatures of 1550 C [2]. For applications in silicon microelectronics, these conditions are hardly viable because they would exceed the melting temperature of the silicon substrate.

On the other hand, pyrolytic deposition of carbon layers by chemical vapor deposition (CVD) is available at temperatures ranging between 350-1200 C depending on precursor gas and deposition conditions [3,4,5]. The physical properties of these carbon layers depend heavily on deposition temperature, carrier gas and residence time of the gas species. While the overall electrical properties of these carbon films cannot directly compete with the idealized

performance of pure graphene or highly-oriented graphite, optimum deposition conditions can be found to achieve a benefit over competing materials (like highly doped poly-Si, TiN, W or silicides) in terms of temperature budget, resistivity, stress and ease of integration.

The mere electrical properties of the pyrolytic carbon layer are as important as their interaction with different interface materials like high-k materials, semiconductors and metals if it comes to integration on a wafer. Some important questions, which need to be addressed, are, how are the properties of the deposited carbon layer? Is there diffusion of carbon or from the interface materials? How does this impair breakdown behavior and reliability in insulating materials? What are the effective work functions for different interface materials? The answers to these questions will lead us to applications of carbon electrode layers in metal-insulator-metal (MIM) capacitor structures, dynamic random access memory (DRAM) capacitors and mid-gap gate-materials, attractive for low power circuits. The question on how these carbon layers interface with silicon will give us in the end powerful low-barrier Schottky diodes that can deal with the high temperature requirements of a front-end process. Therefore, for the first time, carbon-silicon Schottky-diodes can be incorporated in a CMOS flow. For through-silicon vias the most cost-effective "via-first" approach was limited up to now to crystal-Si or poly-Si approach due to the high temperature requirement. Pyrolytic carbon can fill very high aspect ratio vias (up to 400) and offer a much better alternative to Si in terms of resistivity, stress and cost. If modifications of the carbon layers can be achieved at reasonable temperatures, the overall resistivity can be dropped down to 10 μΩcm, which makes it already attractive for competition with W and Cu wiring. The study of maximum possible current densities in the carbon layers results in the finding of a new non-volatile memory based on the conductivity of different carbon configurations. This will not only enable cross-point memory architectures but could also be implemented for configuring field-programmable gate arrays (FPGAs).

Finally, the spin transport properties of carbon may be beneficial to solve the problems of high current densities in spin-torque magnetic memories and for the ubiquitous giant magnetoresistance (GMR) sensors where Neel coupling limits the sensitivity.

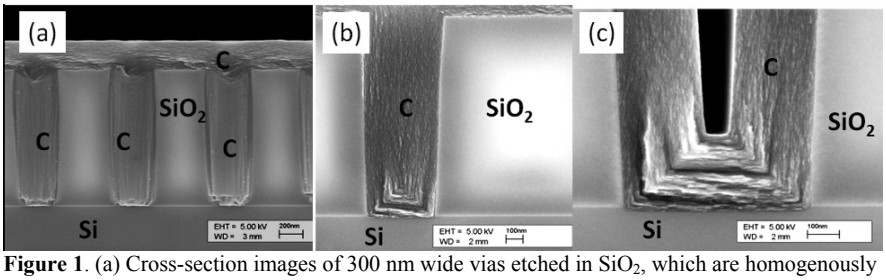


Figure 1. (a) Cross-section images of 300 nm wide vias etched in SiO_2, which are homogenously filled with the highly conductive carbon layer. (b) Shows a zoomed-in image of a single via where the layered structure of the carbon becomes visible. (c) Illustrates a partially filled via and the cross-section prepared by breaking of the wafer details the layered structure of the carbon filling.

EXPERIMENT

The highly conductive, pyrolytic carbon layers are deposited by a pyrolytic CVD process with carbon containing gases (acetylene, methane) in a batch process with many wafers in parallel or as individual wafers as described in reference [3,4,5]. A typical example of the carbon film is given in figure 1 where 300 nm wide vias, which have been etched into a SiO_2 dielectric layer, have been filled homogeneously with the highly conductive carbon film. The highly conformal deposition is a result of the surface-limited reaction of the deposition process.

In order to investigate the filling properties of the deposition process, very high aspect vias with an aspect ratio of ~400 have been used to demonstrate the ability of this carbon deposition process to fill very high aspect structure features. The vertical holes with a depth of 400 µm and width of 1 µm have been produced by my colleague Volker Lehmann by electrochemical etching of a silicon substrate under appropriate conditions. The pyrolytic carbon used for these experiments was deposited at 950° in a hot wall tube furnace using a methane precursor diluted in hydrogen at a pressure of 300 mbar. The samples were heated up in the hot wall furnace in hydrogen atmosphere and cooled down in nitrogen ambient flow. The deposition time depends heavily on the "open area", i.e. the surface area which needs to be coated, but the typically deposition rate can be as high as 10 - 60 nm/min.

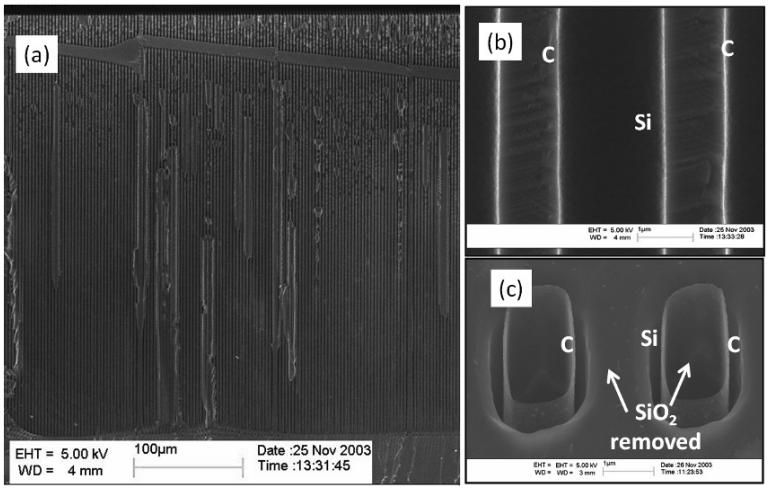


Figure 2. (a) Cross-section of a capacitor structure consisting of a Si-substrate with 400 µm deep and 1 µm wide holes with carbon electrode filling. A zoomed-in image is given in (b) and a short etch in KOH separates more detailed the individual components in this carbon-insulator-silicon structure in (c), where part of the silicon and the SiOx layer are recessed and the carbon filling - practically not etched- is protruding from the surface.

As can be observed in figure 2, this deposition process is capable of filling structures with aspect ratios exceeding 400 almost completely within minutes. Figure 2 shows a cross-section of a Si-wafer in which 400 µm deep and 1 µm wide holes have been etched and subsequently filled with the conductive carbon layer. Several applications can benefit from this behavior:

- High density metal–insulator–metal (MIM) capacitors which can replace discrete components in analog or RF applications
- DRAM-capacitors in trench and stack applications
- Through-silicon vias (TSV) which can enable 3D package with thermal and electrical vias and flexible backplanes for heterogeneous IC integration
- High-aspect ratio contact holes or vias
- Low contact resistance contact material to silicon and SiC

For the first two applications the introduction of high-k is challenging as many high-k materials are not completely mature for CMOS integration and, depending on the process design, a thermal budget over 1000 C is sometimes required for shallow-trench-isolation (STI) or device activation. As will be shown in this paper, pyrolytic carbon is ideally suited for this application due to its high thermal stability and compatibility to high-k and silicon-based dielectrics even after high thermal budget, good conducting properties, and lower process cost than the more established metal-based metallization schemes. This kind of carbon filling has also wide-ranging applications in TSV-interconnects where the filling depth is around 40 – 60 µm, which is roughly the die thickness after polishing the wafer's back side. During backside chemical mechanical polishing (CMP), the carbon pillars serve as an excellent CMP etch stop. As carbon easily withstands temperatures up to 1200 C, a cost-effective via-first approach for TSVs with metal-like electrical conductivities can be established.

DRAM and MIM capacitors

Scaling the DRAM cell to ever smaller technology nodes while maintaining the required 20-30 fF per DRAM cell is a very challenging task and very high aspect ratio capacitors need to be created for both stack- and trench cell concepts. Some melioration can be achieved by the introduction of high-k dielectrics. However, for trench-based DRAM, the introduction of high-k is much more challenging due to the formation of the capacitor prior to device fabrication, which requires STI formation with peak temperatures over 1000 C. For the application in trench capacitors, it is mandatory that the capacitance structure does not deteriorate by high leakage currents, lower breakdown voltages or loss of k-value after a thermal stress.

In earlier technology nodes, poly-silicon has been used to fill the high aspect ratio deep trench, but as scaling continues, this is no viable option anymore as depletion-layer effect in highly doped silicon reduces the capacitance and the overall resistance of the poly-electrode is not acceptable any more. The carbon electrode allows for a higher electron density during positive bias and yields a capacitance increase of 10-20% due to the missing depletion effect in this metallic-like carbon. Another benefit is a reduction of the leakage current by the higher work function of the carbon electrode compared to poly-electrode. The work function of the carbon depends on the deposition method and can be adjusted within some range. In the case of lightly nitrogen-doped carbon, the work function is around 4.41 eV and gives therefore an improvement of 0.3 eV compared to a highly n-doped poly-silicon. The poly-Si fill into the trench is a time consuming process, which can last up to 10 hours due to the complicated diffusion process and

the high doping which needs to be added. The carbon filling process can fill the trench within 10 minutes – which is a huge productivity advantage [3,4]. Figure 3 gives an example of a 6 µm deep trench, which is filled with highly conductive carbon within a few minutes processing time. Detailed evaluations, as shown in figure 3(d), demonstrate that the deep trench resistance can compete with TiN metallization. The trench resistance, measured from the top of the trench to the bottom, is an important part of the RC-time of the trench capacitor and relates directly to the speed with which the capacitor can be charged. In advanced nodes the poly resistance would lead to 100 kΩ resistances and with TiN or carbon, this value can be brought down to the 20 - 30 kΩ range again.

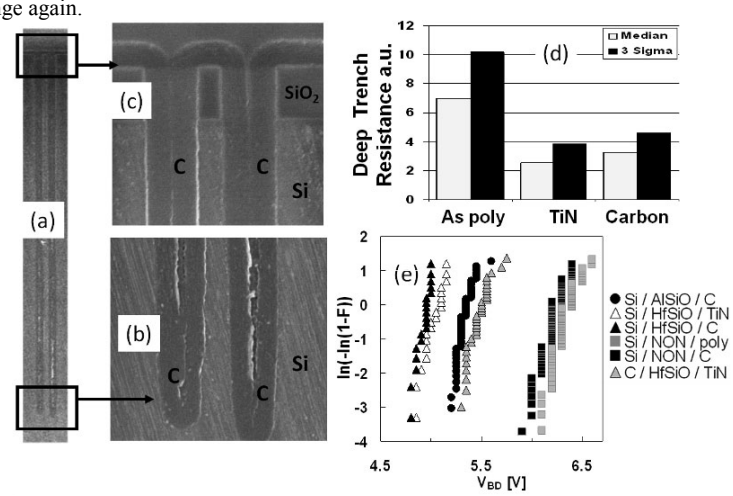


Figure 3. Cross-section of a 6 µm deep trench filled with carbon as conducting electrode. A blow-up off the upper part is shown in (c) and the bottom of the trench is show in (b). The deep trench resistance is compared to TiN and highly doped poly-Si in (d) and the reliability distribution of the breakdown of different capacitor electrodes are plotted in (e) [5].

The lower breakdown voltage in the distribution of figure 3(e) in case of carbon electrode compared to poly electrode comes due to a difference in the work function of the two electrodes. This difference causes a shift in the flat-band voltage and this results an increased electric field across the dielectric for the case of carbon electrode compared to poly electrode for the same applied voltage. In the case of a MIM structure, the depletion effect is missing on two sides of the high-k dielectric, which increases the field even more and causes a further reduction of the breakdown voltage. Although the use of carbon results in lower breakdown voltages compared to poly, there exists a large margin for the product conditions even with the carbon-insulator-carbon (CIC) structures to guarantee a 10 year lifetime. The properties of different approaches of carbon as DRAM electrodes have been already published extensively [5, 6] and have even led to the successful integration into the products based on 58-nm deep trench DRAM technology at Qimonda.

It should be emphasized that the concept of the DRAM capacitors may easily be extended to embedded on-chip capacitors and the compatibility of the carbon electrode with a wide range

of high-k materials can enable better capacitors. An example of such a CIC-capacitor is shown in Figure 4, where carbon is used on both sides of a high-k material based on AlOx in short, only 2.6 µm deep trenches. The 10 - 17 nm thick carbon layer on both sides of the dielectric is in turn contacted by highly doped crystal silicon on the outer side and with poly-Si in the trench hole. The trench could of course be filled completely with the more conductive carbon layer, but in order to allow further processing in a production fab, the carbon has been covered with the well-known poly-Si. This avoids the intricate contamination protocols, which are usually required if "new materials" are introduced into a semiconductor production line and interfaces the subsequent process steps with the well-established poly-Si surface.

The contact between the crystalline silicon and the carbon is achieved by growing carbon on Si. On the inner side of the trench, poly-Si is grown on the carbon surface. The C-Si combination can only be used because the Schottky-barrier of the C-Si contact is reasonably low – a property which we will use to fabricate excellent Schottky diodes – and therefore allows a fast charging and discharging of the capacitor, which is required for fast operation and transient filtering. In order to get a low contact resistance at the C-Si interface extreme care must be taken to maintain a very high surface doping of the silicon on one side and omitting the existence of a thin nitride or oxide layer during the preparation and growth of the carbon layer. If poly-Si is grown on carbon, adequate care needs to be taken for the preparation of the carbon surface, because any porous low-density carbon surface will lead to the formation of a SiC-like layer which would result in an insulating, high contact resistance. The properties of the carbon surface are mainly determined by the way the growth process is terminated and which kind of gas is used to cool down the wafers after deposition. Any preceding wet-chemical treatment, in combination with the atmosphere during the heat-up for poly-Si deposition can induce a thin low-density carbon layer, which would result in SiC formation and an increased contact resistance. However, careful processing allows for a reasonably low contact resistance, so that the silicon-carbon material system can be used.

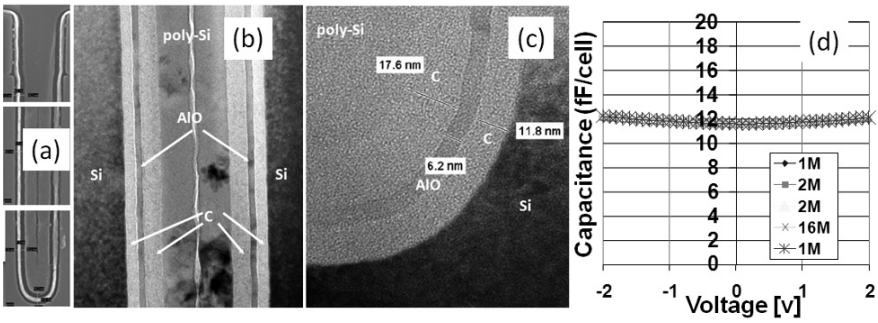


Figure 4. Carbon-Insulator-Carbon (CIC) capacitor fabricated with an AlOx-based dielectric. The cross-section of a short, 2.6 µm deep trench is shown in (a) on the top, middle and bottom of the trench. TEM images of the middle portion are shown in (b) and (c) give a detailed image of the bottom part of the trench CIC. The metal-like, voltage-independent capacitance is plotted for 1M to 16M cells in (d).

The bias voltage dependent capacitance per trench cell for array sizes varying between 1M and

16M is plotted in figure 4(d). It shows attractive metal-like, voltage-independent capacitor properties. A capacitance density of roughly 300 fF/μm^2 can be achieved with this design, outpacing the 3fF/μm^2 obtained for usual SiN MIM capacitors by a factor of 100. However, detailed frequency-dependent measurements of capacitor linearity still need to be done.

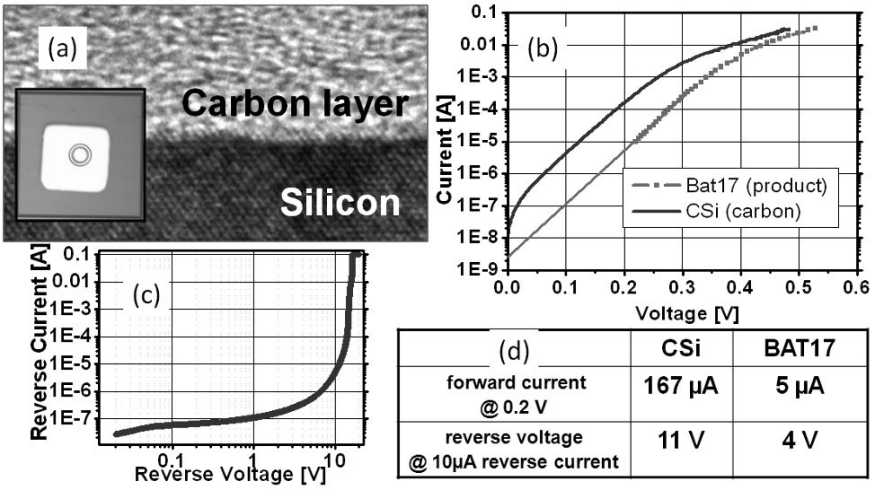
Carbon-Silicon Schottky Diodes

Schottky diodes have the advantages of low forward voltage drop and fast switching speed. Due to their excellent high frequency performance, they are widely used in filter applications for clamping and clipping supply voltages, reverse polarity protection, in mobile phones as network detectors, as WLAN detectors, in 24GHz radar, RFID and other very high frequency mixer applications. In fact, every frequency multiplier operating at over 100 GHz has a Schottky diode as a central element. In order to increase performance, decrease the supply voltage and packaging costs, it would be advantageous not to have Schottky diodes as separate chips on a board but to be able to integrate Schottky diode into monolithic CMOS design. However, Schottky diodes are fabricated by depositing metals on n-type semiconductor materials such as Si, GaAs and SiC and these metal–semiconductor contacts, and consequently the Schottky barrier height, are very sensitive to process and the temperature budget. The properties of the formed silicide contacts vary considerably with process conditions and so would the properties of the diode. The variation is evident even for the standard products, and can be observed in the product specification sheet of different suppliers.

Here we will show that a carbon-silicon (C-Si) Schottky diode has outstanding electrical performance and is high temperature stable - a fact that helps to increase the peak current compatibility [4] and facilitates the integration of this diode into more complex chips. The high temperature stability allows multiple temperature cycles without compromising the diode performance and therefore the diode can withstand complex processes as required for CMOS fabrication. Regular metal-based Schottky diodes cannot withstand high peak currents and temperatures because the metal diffuses into the Si base layer and destroys the diode properties.

In order to perform a direct benchmark with a commercially available product we used a BAT17 Schottky diode vehicle where substrate, all layouts, doping levels and guard ring implants have been kept the same as the commercial product, but instead of having the standard metallization for the formation of the Schottky contact, we used the carbon-layer to establish the Schottky contact. A thin metal layer consisting of 5nm Ti and 20 nm Au was deposited on the 100 nm thick carbon by a shadow mask and this metal layer served as an etch mask to remove the carbon layer from the open area, so that the deposited carbon contacts only the active silicon area. The inset in figure 5 (a) gives a top view photograph of the device with circular diode active area and the TEM image shows the atomically resolved carbon-silicon interface. The forward currents of the diode with metal silicide (Bat17) and with carbon are plotted in figure 5 (b). The C-Si diode delivers over 15 times more current at a given voltage due to its lower Schottky barrier, which has been evaluated by the Norde-plot to be 0.41 eV for n-doped and 0.59 for p-doped silicon. The ideality factor for the diodes is 1.1 and and higher ideality factors could be correlated with the presence of an oxide at the interface, which could grow during non optimized heat ramps. At current levels above 1 mA, the missing metallization for the C-Si diode leads to an increased serial resistance caused by current crowding at the small measurement area from the probe tips, whereas the product BAT 17 is packaged and wire-bonded. Interestingly enough, the reverse leakage at low bias is higher for the C-Si diode, but lower than the BAT17

diode at higher reverse voltage. As summarized in figure 5(d), this means that the blocking voltage of the C-Si is 11V instead of only 4 V as for the BAT17 diode at a specified leakage current of 10 µA. The leakage current increase at low voltages is a direct consequence of the lower Schottky barrier height and can be explained by this. On the other hand, the field at the edge of the diode, where the guard ring is, is much higher for the silicided contact, because the silicidation process consumes a bit of silicon and leads to a very sharp metallic edge feature. The field enhancement at this edge leads to an earlier breakdown at higher voltages. In contrast to this, carbon does not develop this sharp feature at the edge, due to the missing silicidation and consequently develops a lower field at the same applied reverse voltage. The observed steep increase of reverse current at 12 V is the breakdown of the reverse biased p-n-junction of the guard ring. The behavior of the diode does not noticeably change even if it is subjected to a 1000 C anneal, which allows the combination with conventional CMOS front-end processes.



(d)	CSi	BAT17
forward current @ 0.2 V	167 µA	5 µA
reverse voltage @ 10µA reverse current	11 V	4 V

Figure 5. A TEM cross-section of carbon-silicon Schottky diode is shown in (a) together with an inset of a top-view photograph of the diode device. The golden Ti/Au metallization on top of a carbon layer serves as an etch mask for the carbon and the circular area is the active diode area with the guard ring. The forward current characteristic of the C-Si diode and the BAT17 product is plotted in (b). The reverse I(V) of the C-Si diode is shown in (c) and a benchmark table comparing C-Si and commercial Bat 17 in (d).

From the direct comparison of the two Schottky-diodes, it is possible to conclude that the capacitance of the diode that is roughly proportional to the junction area can be reduced by a factor of 15 while maintaining the same current drivability, if one is using the C-Si contact. This has important consequence in high-speed applications because the switching speed is impacted by this capacitance. The C-Si interface is capable of withstanding current pulses in the order of 30 MA/cm^2 without deterioration, which is very interesting for filter applications. There are also applications in non-volatile resistive memories that can benefit from a diode with high drive