CAMBRIDGE

Cambridge University Press
978-1-108-49845-6 — Fast Techniques for Integrated Circuit Design
Mikael Sahrling
Index
More Information

Index

2-pi-models, 104

active cascode, 34
ADC *see* analog digital converters
ADC model
  basic, 196
  sampling, 199
Ampere's law, 54, 61, 75, 77
amplifier stages
  basic level, 4
  cascaded, 44
  higher level, 31
analog digital converters, x, 195
architectures
  ADC, 201
  PLL, 171

back of the envelope calculations *see* estimation analysis
bandwidth
  estimate, 42
basic PLL equations, 175
basis functions, 162
bipolar, 4
bit error rate, 39, 41
  calculation, 38
  definition, 203
body effect, 4, 235
boundary conditions
  derivation of, 61

capacitance
  calculating, 66
  definition of, 65
  fringe, 28
  one dielectric media, first principle calculation, 68
  simple calculation, 68
  two dielectric media, first principle calculation, 70
capacitor
  circuit element, 67
  serial formula, 72
cascode, 21–22, 28, 31, 33
  active feedback, 33
CD stage, 7, 10
  with resistor capacitor ladder load, 16
CG stage, 5
characteristic impedance, 107–108, 116
charge sampling
  theory, 222
circuit analysis *see* circuit theory
circuit design, 30, 49–50, 85, 90, 101
circuit theory, ix, 51, 109
CMOS inverter
  cross-coupled, 25
  single, 23
CMOS transistor
  inherent gain, 14
  small geometry bandwidth, 10
  small geometry current, 182
common drain *see* CD stage
common gate *see* CG stage
common source *see* CS stage
comparator, 34, 41
  no output load, 40
comparator design, 45
conduction current, 54
conformal coordinate transformation, 95
conformal transformations, 93, 96
continuity equation, 54
convolution theorem, 216, 221
co-planar wave guides, 103
Coulomb gauge, 53
CS stage, 8, 15
current distribution
  perfectly conducting ground plane, 87
  related to inductance, 66
  resistive ground plane, 89
  thin conductors, 93
current mirror, 20
current sheet over ground plane
  first principle calculation, 82
cylindrical symmetry, 2, 58, 74, 76, 85

Delta gap source, 161
design examples, 4, 31, 122, 166, 234
design phase, 3

© in this web service Cambridge University Press www.cambridge.org

CAMBRIDGE
Cambridge University Press
978-1-108-49845-6 — Fast Techniques for Integrated Circuit Design
Mikael Sahrling
Index
More Information

differential nonlinearity (DNL), 202
differential pair, 18
Dirac delta function
  definition of, 213
distortion, 15, 17, 199, 202, 209
distributed effects, 102

effective number of bits (ENOB), 203
effective radius
  using adjacent circular segments, 126
  using area equivalence, 127
  using maximum length scale, 128
EFIE, 160
electric field integral equation *see* EFIE
electrical length, 108–109, 116, 134
electromagnetism, ix, 50, 101
estimation analysis, 1
estimation calculations, ix
evaluation, 3

field energy, 63
  electrical, 63
  magnetic, 64
fine tune, ix, 3, 191, 194, 207
first principles, ix, 68, 85
five transistor amplifier, 31
Flash ADC, 201, 206
foundry supplied inductor libraries, 104
Fourier transform
  sample and hold signal, 218
  track and hold signal, 218
  track phase, 217
Fourier transform, 212
full scale voltage, 38, 41
full wave approximation
  single frequency, 54

Galerkin's method, 160
gate impedance, 6–7
gauge choice, 53
gauge invariance, 52
gauge potentials, 52–53, 94
gauge symmetry, 53
Gauge theory, 52
gauge transformation, 53
Gauss' law, 62–63
  definition of, 239
Green's function
  1D, 58
ground planes, 102

hand calculation *see* estimation analysis
Helmholz equation, 56–60, 84
high frequency phenomena, 85
high speed integrated circuit
  size of modern, 102
homogeneous equation, 56

ideal impulse sampling, 221
ideal sampling switch, 214
impressed current, 54
impulse sampling, 215
impulse sensitivity function, 187, 189
inductance
  calculating, 73
  definition of, 65
  single straight wire, 74
  single wire over ground plane, first principle calculation, 79
  two straight wires, first principle calculation, 74
inductors as circuit elements, 73
initialization phase
  comparator, 35, 42
input impedance, 5–9, 23–25
input pair, 35, 39, 42, 45, 49
input stage
  comparator, 8, 38, 40, 42, 45, 201
  Flash ADC, 207, 209
input transistors *see* input pair
integral nonlinearity (INL), 202
integrated circuits, 4, 53, 56, 70, 101, 119, 122
inter symbol interference (ISI) *see* Jitter:inter symbol interference
interleaving adc, 203
inudctor model including
  parasitic capacitand and resistance, 135

jitter, ix, 3, 165–168, 170, 184, 203, 211, 224, 226–231
jitter, 166, 230
  anti-correlated, 227
  correlated, 227
  data-dependent, 166
  deterministic jitter, 166
  duty cycle distortion, 166
  Gaussian, rms, 166
  inter symbol interference, 166
  periodic, 166
  random, 166
  uncorrelated, 229
  uncorrelated bounded, 166
  vs phasenoise, 167

KCL *see* Kirchoff's current law
Kirchoff's current law, 5

Laplace equation, 93
lateral skin effect, 97, 100, 137, 148
LC-VCO, 149, 191
linearization techniques, 4
linearize, 2, 4–5, 21, 175
linewidth, 171
lithography, 102
load resistance, 25, 48

© in this web service Cambridge University Press www.cambridge.org

CAMBRIDGE
Cambridge University Press
978-1-108-49845-6 — Fast Techniques for Integrated Circuit Design
Mikael Sahrling
Index
More Information

long wavelength
  approximation, 55
  simulators, 152
loop equations, 26
Lorenz gauge, 53

machine learning, 104
magnetic charges, 52
magnetic field integral equation *see* MFIE
Matrix equation, 160
Maxwell's equations, 51, 66–68, 70, 73–74, 85
  1D – solution, 56
  2D – solution, 58
  3D – solution, 59
  external sources, 54
  solutions, 56
metal-insulator-metal capacitor *see* mim capacitor
metastability, 38
method of images, 80
method of moments, 159
MFIE, 160
Miller effect, 9, 27–28
MIM capacitor, 119
MOM capacitor, 121
multi-layer ground planes, 103

narrow-band applications, 8
negative resistor, 7–8, 16, 185
noise analysis, 31, 48
noise optimization, 45
noise transfer, 20, 31–32, 41, 171, 219
nonlinear effects, 4
nonlinear extension, 9, 29
  CD stage, 10
  CS stage, 15
nonideal sampling switch, 219
Nyquist criterion, 199

offset, 202
Ohm's law, 93
one turn inductor, 129
output conductance, 12, 14, 31

Parseval's theorem, 168, 170
  definition of, 239
partial inductance, 122–123
partial inductance of a wire stub pair, 122
PCB
  connection to IC, 102
performance criteria
  adc, 202
  PLL, 172
permeability, 51
permittivity, 51, 55, 70, 72, 85, 102, 136, 139, 234
perturbation analysis, 4
phase locked loop (PLL), ix, 171
phase noise, 187
phenomenological model, 135, 138
pill box, 61
pi-models, 104
pipeline converter, 201
PLL *see* phase locked loop
Poisson equation, 57, 58
positive feedback, 38, 43, 184
potential field, 52, 152
power, 202
printed circuit board (PCB), 102
propagation constant, 106
propagation delay, 23

Q - quality factor
  definition of, 138

rectangular cross section, 126
regeneration phase
  comparator, 37, 42
regularization theory, 104
reset, 35, 40–41, 45, 207
reset phase
  comparator, 35
reset switch, 207
reset switches, 40, 45
RF performance, 104

sampling
  finite pulse width, 222
sampling rate, 41, 199–201
saturation, 5, 16, 23, 27–28, 236
scaling relationships, 42
self-resonance, 134
shielding techniques, 1, 101
sigma-delta converter, 201
signal integrity, 103
signal-to-noise and distortion ratio (SNDR), 202
signal-to-noise ratio
  definition, 202
simple straight wire in free space, 74
simplification, 2
simulation, 12, 15, 46, 81, 125, 131–132, 134, 137, 151–152, 161
simulators, 87, 151
  principles, 151
single transistor gain stages, 4
skin depth, 85
small geometry CMOS, 23, 28, 87, 102, 121
SNR, 41, 166, 198, 200–203, 206, 208, 227–229, 231
  improvement using averaging, 200
S-parameters, 101, 109, 112–114, 116–117
  definition of, 109
spurious-free dynamic range, 203
stability, 176
  feedback systems, 176
Stoke's theorem, 61, 76–77
  definition of, 240
strong-arm comparator *see* comparator

© in this web service Cambridge University Press www.cambridge.org

CAMBRIDGE

Cambridge University Press
978-1-108-49845-6 — Fast Techniques for Integrated Circuit Design
Mikael Sahrling
Index
More Information

substrate resistance, 136
substrate resistivity, 137, 234
Successive Approximation Register (SAR), 202
surface charge, 63
surface current, 62

Taylor expansions *see* Taylor Series
Taylor series, 10
third harmonic
  differential pair, 19
through-silicon-vias (TSV), 104
time domain, 25, 31, 42, 184, 189, 223
time evolution, 37
time-digital converter, 201
time-interleaved converters, 202
timescale/s, 27, 31, 35–36, 38, 40–43, 45, 48, 234
total harmonic distortion (THD), 202
track and hold, 216, 218
transconductance, 32
transfer function, 10, 15, 17, 25, 29, 171, 175–176, 178, 181–182
transition frequency, 6
transmission lines, 101
  basic theory, 105
two transistor stages, 18
two-turn inductor, 129, 134, 137, 144
two-dimensional solution, 58
two-pole system, 9, 177

VCO
  active design, 193
  frequency of oscillation, 184
  performance criteria, 183
  steady state amplitude, 185
  tank design, 191
vector potential, 52, 56, 60, 66, 76–77, 83, 94, 123, 155, 161
verification, 3
vias, 103
voltage controlled oscillator *see* VCO
voltage field *see* potential field
voltage sampling theory, 211
Volterra series, 9
volume charge, 63
volume current, 61

wavelength, 53, 55, 57, 60, 68–69, 84–85, 88, 93–94, 101–102, 108–110, 117, 151–152, 159

© in this web service Cambridge University Press www.cambridge.org