1 General Guidelines in Estimation Analysis in Integrated Circuits

Learning Objectives

- Definition and overview of estimation analysis flow.

1.1 Introduction

This chapter provides a summary of steps needed to make useful mathematical models of physical systems. I refer to these steps as "estimation analysis" but in hallways of science and engineering schools or engineering offices they are often referred to as hand calculations or back-of-the-envelope calculations. I am not a big fan of these terms, as they convey a sense of sloppiness, which is far from accurate. This type of analysis is useful for building deeper understanding of integrated circuits and systems, but the methodology is very general and can be applied to most systems governed by some kind of mathematics. From deep space astrophysics to microscopic systems such as integrated circuits you will find broad applications of this kind of thinking. With this broad applicability it is no surprise that the principles we outline here are somewhat vague, but we will discuss enough examples in the rest of the book to enable the reader to develop a good sense of how to proceed in different situations. A mastery of these ideas will only come with experience. The process can be time-consuming initially because it involves digging into the core of the system under consideration. If the system is new to the user, the learning process can take even longer. But oftentimes, and with practice, the systems are similar enough to other systems the user has seen before that the process can be quite swift. We will start by outlining the principles and then discuss each of them in some depth. We will then refer to these steps in the following chapters, where many examples are provided.

After a model has been developed one can use it as a starting point for fine-tuning in a simulator or on the bench or whatever might be practical.

1.2 Principles

A beginner often tries to solve a problem with brute force, using three dimensions, full nonlinear equations, etc. The problem will then quickly become intractable with

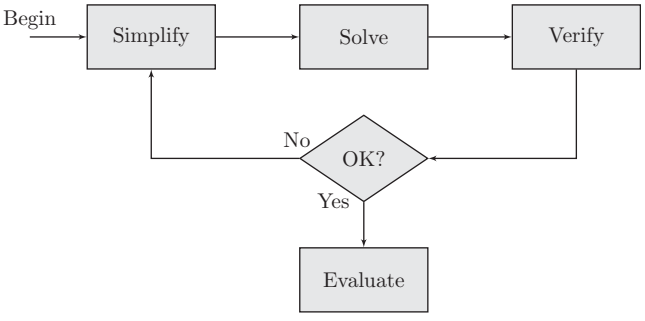

Figure 1.1 Estimation analysis work flow.

myriads of sums and complex expressions yielding little insight. With experience one learns that the core behavior is often much simpler to catch but it requires thinking the problem through before full calculations start. For the novice this can often be frustrating but with practice one learns to see the value of this approach.

In a typical modeling situation there are four steps to follow:

(1) Simplify – This is often the most difficult step because it attempts to get to the core of how the system works.
(2) Solve – If step 1 is executed properly this will be relatively easy.
(3) Verify – Here we verify the solution in step 2 is correct by for example checking extreme cases and/or comparing to simulations and/or exact calculations. If something is wrong, go back to step 1.
(4) Evaluate – In this section we analyze what the solution means.

We will discuss each of these in turn: see Figure 1.1 for a simple flow diagram.

Simplify

To properly simplify we need to be able to understand what we actually want to know. Is it a length scale, gain, bandwidth, linearity, etc.? How can we simplify the system so that this property will be highlighted? Can we make it two-dimensional, one-dimensional, cylindrical symmetry, spherical symmetry, planar symmetry? Can we linearize it? If we are interested in gain or noise, linearization is a great technique. Perhaps a harmonic tone is causing headache and perturbation calculation is in order? If we are looking at a clocked system, perhaps an ideal switch with infinite edge rate will suffice?

Solve

This often involves fairly simple algebra. In some cases there are some useful mathematical techniques available and in this book we will describe them as we move along and for more complex techniques we will refer to the literature.

Verify

This step is often neglected in practice but it is critical. If we have missed something essential in the model, the behavior of the model will simply be wrong and we will not have learned what we set out to learn. Oftentimes one can find similar calculations in the literature that can be used for verification. At other times one can simulate to confirm that the model fully captures the desired properties. This simulation is not to be used as a substitute for understanding, but to confirm the model assumptions and calculations are correct. A good technique is to take various parameters and go to the extremes to make sure the behavior is as expected. For example, if we are investigating the gain of an amplifier with a degeneration resistor, does the model go to the correct limit when this resistor is zero or infinite?

Evaluate

What does the solution mean? Is there something one can do with a certain variable combination that will result in something useful, like improved jitter or reduced power? If we need smaller inductance, will widening the metal width be efficient?

Most education comes with experience. The road is narrow and sometimes long but it is a great journey and the joy of understanding something on a deeper level cannot be overstated.

In this book we will illustrate estimation analysis methodology by going through many specific examples to showcase what can be done. My hope is that the reader will be inspired to go well beyond what is described here and invent great things. We will do simple circuit analysis that most readers will already be familiar with and then move on to complex examples such as the direct solution of Maxwell's equations and system analysis of analog-to-digital converters (ADCs) and phase-locked loops (PLLs). We will also discuss deeper physical concepts such as the nature of jitter and its relationship to phase noise.

1.3 Integrated Circuit Applications

Having established a simple model we can proceed to the design phase by applying the model to a specific design problem. We derive a set of parameters such as transistor sizes, interconnect width, etc. and use those as a starting point for the design in the simulator. The idea is to use the simulator to fine-tune the design. We should already know, within the accuracy of the simple model, what to expect from simulation. This kind of approach presents a huge shortcut in the design effort.

In this book we will build various models and use them in real-world design examples to establish a good starting point for fine-tuning in simulators.

2 Basic Amplifier Stages

Learning Objectives

- Applying estimation analysis to basic amplifier stages
  - Linearization techniques – amplifier gain and impedance
  - Perturbation analysis – weak nonlinear effects

2.1 Introduction

In this chapter we introduce basic transistor amplifier stages and use them as a starting point to describe the estimation analysis method. For more details on the transistors and the models used we refer to Appendix A.

For the reader familiar with the discussion in books such as [1–5] this chapter should not pose any difficulty.

Fundamentally, all we do in all these simplifications is to linearize the transistor or amplifier at its bias point and draw conclusions about fundamental properties such as gain and impedance. We ignore the body effect for clarity, by assuming that the body is always tied to source in all transistors.

In addition, we will also venture into the world of weak nonlinear effects and show how these gain stages can be analyzed with simple extensions to the standard linearization techniques, all in line with the estimation analysis method.

We start the chapter with a section on single transistor gain stages and continue with a few well-known two transistor stages. For brevity, we will focus on CMOS transistors, but other transistor types such as bipolar can easily be analyzed in the same way. We go through some design examples in detail in order to use the results in the later chapters.

2.2 Single Transistor Gain Stages

Single CMOS transistor gain stages are traditionally divided into three groups: common gate (CG), common drain (CD), and common source (CS) stages. The word common refers

to the terminal that is common to both input and output signals, which can be either voltage or current. We will describe them one by one in this section. We will keep the discussion at a general level; the precise expression for the currents' dependence on terminal voltages does not matter. Only in the final expression, when we are after something specific, do we use specific current voltage relationships described in Appendix A.

CG Stage

The common gate (CG) stage is an amplifier where the gate node is tied to a fixed voltage, possibly with some impedance in series. The input signal enters through the source terminal and exits at the drain terminal. The signal is best described as a current.

Here we will solve for gain and input impedance.

Simplify We assume the transistor is in saturation so we will ignore the drain gate capacitance. We also assume the drain source impedance is sufficiently large so as not to affect the gain; and finally we assume the output load to be zero ohms. The transistor model in Figure 2.1 shows our assumptions. When comparing with the literature this could be seen as an over-simplification, but we are only interested in the dominant parameters that set the gain and input impedance so that the simplifications are an adequate approximation for an estimation analysis. To calculate the gain we will in addition linearize the transistor around its bias point.

We find for $Z_G = 0 \rightarrow v_g = 0$ and by applying Kirchoff's current law (KCL) at the output node

$$i_{out} = g_m \left(v_g - v_s\right) = -g_m\, v_s.$$

We also know

$$i_{in} = -v_s j\omega C + i_{out}.$$

Solve By solving for v_s we find

$$i_{out} = -\frac{g_m(i_{out} - i_{in})}{j\omega C},$$

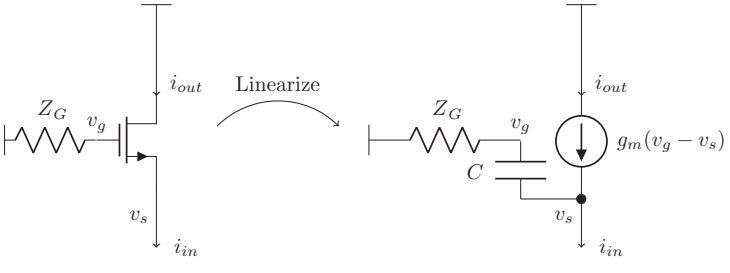

Figure 2.1 Common gate transistor stage with linearization.

or

$$\frac{i_{out}}{i_{in}} = \frac{g_m/j\omega C}{(1 + g_m/j\omega C)} = \frac{g_m}{(j\omega C + g_m)}.$$

We see for low frequencies that the input current goes straight through to the drain or output, but for higher frequencies the capacitor between the gate and the source will act as a short, effectively grounding the current and leaving nothing to the output. The transition point where $|j\omega C| = g_m$ is a rough estimate of the transition frequency or f_t. A more detailed model can be found in [3]. Here we get

$$f_t = \frac{g_m}{2\pi C}. \tag{2.1}$$

This is an important figure of merit for high speed designs and the expression (2.1) is a convenient rule of thumb.

What about the input impedance? We now have to rewrite i_{in} in terms of v_s:

$$i_{in} = -v_s j\omega C + i_{out} = -v_s j\omega C - g_m\, v_s = -(j\omega C + g_m)\, v_s.$$

We find

$$Z_{in} = -\frac{v_s}{i_{in}} = \frac{1}{j\omega C + g_m}.$$

Imagine now there is a gate impedance, Z_G. We find

$$v_g = -\frac{1/j\omega C}{1/j\omega C + Z_G} v_s + v_s = \frac{j\omega C\, Z_G}{1 + j\omega C\, Z_G} v_s,$$

or

$$i_{out} = g_m\,(v_g - v_s) = -g_m \left(\frac{1}{1 + j\omega C\, Z_G}\right) v_s.$$

To find the input impedance we need to rewrite i_{in} in terms of v_s.

$$i_{in} = (v_g - v_s) j\omega C + i_{out} = -\left(\frac{j\omega C + g_m}{1 + j\omega C\, Z_G}\right) v_s.$$

We the find after a simple rearrangement

$$Z_{in} = -\frac{v_s}{i_{in}} = \left(\frac{1 + j\omega C\, Z_G}{g_m + j\omega C}\right).$$

Verify As the reader no doubt recognizes, these calculations can be found in any standard electronics book, but here we have made some simplifications beyond that which is normally done. This is all in line with the estimation analysis idea. We are only seeking a model that is simple enough to capture the essence of what we want to know, in this case gain and input impedance. The calculations in this chapter are easy to verify in the literature. We will encounter more complex situations in Chapters 4–7.

Evaluate We have followed the estimation analysis method and we recognize the calculations from similar examples in the standard literature. To investigate the meaning

of these expressions we need to go to various limits of key parameters. This is also often a way to sanity check the answer.

Let us look at the gain

$$A = \frac{I_{out}}{I_{in}} = \frac{g_m}{(j\omega C + g_m)}.$$

If $\omega \to 0$ we see the gain $A \to 1$. For high frequencies, $\omega \to \infty$ we see the gain $A \to 0$. Obviously, when $g_m \to 0$ the gain $A \to 0$.

Similarly, for the input impedance

$$Z_{in} = \left(\frac{1 + j\omega C\, Z_G}{g_m + j\omega C}\right).$$

We see an interesting relationship between the gate impedance and its reflection at the source. When $\frac{\omega}{2\pi} \ll f_t$ the gate impedance will be rotated by 90 degrees so a resistor in the gate will look like an inductor at the source, a capacitor will look like a resistor, and, most disturbingly, an inductor will look like a negative resistor, a kind of gain that can cause instabilities. For the limit $\omega \to 0$, the input impedance is simply $1/g_m$. In the other limit, $\omega \to \infty$ the input impedance is simply Z_G, which makes sense since in this case the gate capacitance shorts the $1/g_m$ from the transconductor.

CD Stage

For the common drain (CD) stage the input voltage goes to the gate of the transistor and the output is picked off of the source. It is often referred to as a source-follower circuit, or follower for short. The basic circuit configuration can be found in Figure 2.2.

We will solve for gain and input impedance.

Simplify First we will simplify the situation in a similar fashion to the CG stage.

Solve The output of the source will look like

$$v_{out} = (i_d + (v_{in} - v_{out})j\omega C)Z_L, \qquad i_d = g_m\,(v_{in} - v_{out}).$$

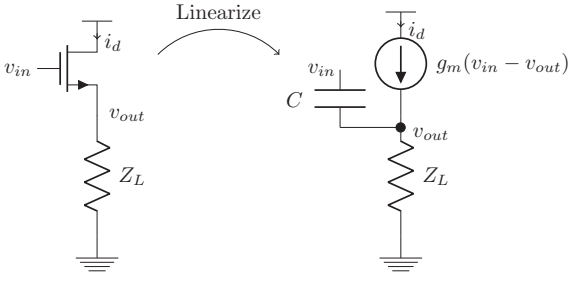

Figure 2.2 Common drain transistor stage with linearization.

After a simple rewrite

$$\frac{v_{out}}{v_{in}} = \frac{(g_m + j\omega C)\, Z_L}{(1 + (g_m + j\omega C)Z_L)}. \tag{2.2}$$

The input impedance is now calculated by getting the input current

$$i_{in} = \frac{v_{in} - v_{out}}{1/j\omega C} = j\omega C\, v_{in} \frac{1}{(1 + (g_m + j\omega C)Z_L)},$$

and rearrange to find

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{j\omega C}(1 + (g_m + j\omega C)Z_L). \tag{2.3}$$

Verify This is again a standard calculation in textbooks see for example [3].

Evaluate Let us look at the expression for gain, equation (2.2). When $\frac{\omega}{2\pi} \ll f_t$ we see

$$v_{out} = \frac{g_m\, Z_L}{(1 + g_m Z_L)} v_{in}.$$

For large load impedances, $g_m Z_L \gg 1$ $v_{out} \to v_{in}$. In the other extreme, $Z_L \to 0$ we get $v_{out} \to 0$, the output is simply shorted to ground.

As in the common gate stage we see the input impedance sees a 90 degree rotation of the impedance at the output, but this time it goes the other way: an inductor looks like a resistor, a capacitor looks like a negative resistor and a resistor looks like a capacitor. In fact for many input stages in narrow-band applications, like cellular phones, this property is a really nice way to create a low-noise input termination with the use of an inductor at the source of the input stage. The input stage will rotate this inductor to look like a real impedance with little noise(!). The remaining capacitor is often resonated out by a series inductor but that is a topic for another book.

CS Stage

The common source stage is perhaps a configuration that one often encounters early on in one's career. A common setup can be seen in Figure 2.3.

We will calculate gain and input impedance again.

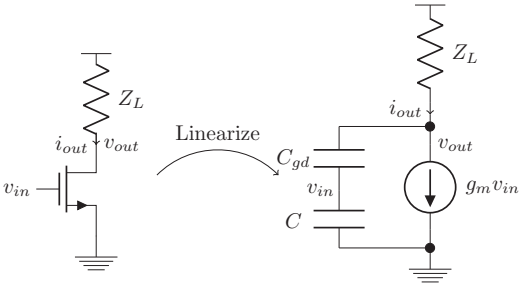

Figure 2.3 Common source transistor stage with output load.

Simplify The output is a voltage when loaded with an impedance and the input is a voltage. We follow a similar linearization technique to that we had before, but this time we will include the gate drain capacitance, C_{gd}. We then have to solve KCL at the drain and source, we assume the gate driving impedance is zero.

Solve We have for the basic parameters

$$i_d = g_m\,(v_{in} - v_s) \quad v_s = 0 \quad i_s = i_d + j\omega C(v_{in} - v_s),$$
$$i_{out} = i_d + j\omega C_{gd}(v_{out} - v_{in}) \quad v_{out} = -i_{out}Z_L$$

We find

$$-\frac{v_{out}}{Z_L} = g_m v_{in} + j\omega C_{gd}(v_{out} - v_{in}) \rightarrow A_{gain} = \frac{v_{out}}{v_{in}} = \frac{j\omega C_{gd} - g_m}{1 + j\omega C_{gd}Z_L}Z_L.$$

The input impedance is

$$Z_{in} = \frac{v_{in}}{j\omega C_{gd}(v_{in} - v_{out}) + j\omega C v_{in}}$$

Upon substitution of v_{out} from the expression of gain above we can rewrite

$$Z_{in} = \frac{1}{j\omega C_{gd}\big(1 - Z_L\big(j\omega C_{gd} - g_m\big)/\big(1 + j\omega C_{gd}Z_L\big)\big) + j\omega C}$$
$$= \frac{\big(1 + j\omega C_{gd}Z_L\big)}{j\omega C_{gd}(1 + g_m Z_L) + j\omega C\big(1 + j\omega C_{gd}Z_L\big)}$$

Verify As before, this is a standard calculation in [2] but here we made even further simplifications to get an estimate of the gain and impedance.

Evaluate We see for low frequencies the gain, $A_{gain} = -g_m Z_L$, but there is a cross-over frequency where the gain transitions at $\omega = g_m/C_{gd}$, in effect the major output current is supplied by the gate drain capacitance C_{gd} instead of the transistor gain. In the literature this is known as a right half plane zero. The input impedance is essentially a two-pole system due to the two capacitors. We see for low frequencies the total capacitance is the sum of C and $C_{gd}(1 + g_m Z_L)$, the gate drain capacitance has been amplified a factor $(1 + g_m Z_L)$. This effect is known as the Miller effect, the gain across a capacitor will amplify the capacitors value, increasing the effective load.

Nonlinear Extension

We can now employ the same technique to examine nonlinear extensions. In general one needs to employ Volterra series for electronics systems instead of the more

commonly known Taylor series. This is due to the fact the systems we are considering have memory in that the output signal depends to some degree on what happened at earlier times in perhaps other parts of the circuit. The simple stages we will look at here have relatively high bandwidth in small geometry CMOS technologies, $f_t > 100$ GHz so we will assume a Taylor series expansion is appropriate. It often turns out to be quite useful, but care must be taken and the important verification step must be completed to make sure we do not fool ourselves and are better served with Volterra series.

For Taylor series we can write the output as a polynomial expansion of the input:

$$I_o = I_o^0 + I_o^1 V_o + I_o^2 V_o^2 + I_o^3 V_o^3 \ldots$$

Here

$$I_o^1 = \frac{dI}{dV}$$
$$I_o^2 = \frac{1}{2}\frac{d^2 I}{dV^2}$$
$$I_o^3 = \frac{1}{6}\frac{d^3 I}{dV^3}.$$

The coefficients can be calculated in several different ways: (1) One can sweep the DC bias point in a simulator and take the appropriate derivatives. (2) One can do a Fourier transform of the output when the input is a single tone sinewave, the linear and higher-order coefficients can be found from the harmonic powers. When relating the two methods keep in mind the mixing effect of the Taylor series when using sinusoids, $V_0 = A \sin \omega t$:

$$I_o = I_o^0 + I_o^1 V_o + I_o^2 {V_o}^2 = I_o^0 + I_o^1 A \sin \omega t + I_o^2 A^2 \sin^2 \omega t$$
$$= I_o^0 + I_o^1 A \sin \omega t + I_o^2 A^2 \frac{1 + \cos 2\omega t}{2} = I_o^0 + I_o^2 A^2 \frac{1}{2} + I_o^1 A \sin \omega t + I_o^2 A^2 \frac{\cos 2\omega t}{2}.$$

For example, the second-order term splits into a DC component and a second harmonic component. To find the size of the second harmonic term one needs to divide the second-order derivative of the transfer function by a factor of four. A factor of two comes from the Taylor expansion and another factor of two from the mixing action, where half the amplitude goes to DC and rest into the second harmonic. This is similar for higher orders but obviously more complex.

CD Stage

We will follow the CD stage discussion and make a first order correction to the gain calculation.

We start with

$$v_o = g_m (v_{in} - v_{out}) Z_L,$$

where we assume the frequencies of interest are far below f_t, and we are using Figure 2.2 for reference. In this section we limit ourselves to gain calculations.