Part I

High Permittivity DRAM Materials
Leakage Degradation in BST Dielectric Capacitors with Oxide and Metal Electrodes

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ABSTRACT

Leakage degradation under DC stresses in epitaxially-grown Ba$_x$Sr$_{1-x}$TiO$_3$/SrRuO$_3$ capacitors with various top electrodes was examined. Epitaxial capacitors employed in this study exhibit higher dielectric constant arising from optimized lattice deformation caused by lattice mismatch between Ba$_x$Sr$_{1-x}$TiO$_3$ and SrRuO$_3$; dielectric constant for SrRuO$_3$/30nm thick Ba$_{1-x}$Sr$_x$TiO$_3$/SrRuO$_3$ all oxide capacitor was 550, which corresponds SiO$_2$ equivalent thickness of 0.21nm. In addition, this type of capacitors have interfaces of higher cleanliness between dielectrics and electrodes, which are expected to provide opportunities of more simplified discussions on reliability issues for thin film capacitors. Dielectric breakdown properties and DC stress-induced leakage degradation properties were examined in room temperature and elevated temperatures. Various kinds of leakage degradation were observed and categorized in anode degradation and cathode degradation. The degradation in capacitors with oxide electrodes was markedly suppressed compared to that in capacitors with metal electrodes such as Pt or Ru. This higher degradation resistance yielded longer lifetime in capacitors of this type and the estimated life time at 458K for SrRuO$_3$/ Ba$_{1-x}$Sr$_x$TiO$_3$/SrRuO$_3$ capacitor was 3E8 seconds, which exceeds required specification for DRAM application. These differences were discussed on the basis of a supposed degradation mechanism in which oxygen vacancy generation at anode interface is taken into account as well as vacancy accumulation at cathode interface.

Introduction

(Ba$_x$Sr$_{1-x}$TiO$_3$)(BSTO) has been an important high permittivity candidate material for post 1-Gbit dynamic random access memories (DRAMs) and a great deal of efforts are concentrated to improve its properties. BSTO capacitor performance such as dielectric con-

![Fig.1. Schematic model for enhanced dielectric constant in artificially distorted epitaxial SrO/BSTO/SrO capacitor: in-plane compressive stress caused by lattice mismatch yields higher dielectric constants.](image-url)
stant, leakage current and degradation resistance, obtained so far is, however, far from what is expected for the actual use in advanced DRAMs. We have developed novel epitaxial BSTO capacitors employing conducting perovskite oxide SrRuO$_3$ (SRO) as bottom and top electrodes, which exhibit an extremely high dielectric constant and very low leakage current$^1$. In addition, these all oxide epitaxial capacitors exhibit a longer lifetime in TDDB tests and less degradation compared with those in conventional polycrystalline capacitors with metal electrodes. Their superior performance is attributed to the appropriate lattice deformation caused by the lattice constant mismatch between BSTO and SRO and the cleanliness of their heteroepitaxial interfaces (Fig.1). These all oxide epitaxial capacitors would be a promising candidate for future DRAM permittivity, as well as they would provide important guidelines to improve initial performance and reliability of more conventional capacitors. In this paper, we report properties of the epitaxial capacitors such as capacitance, leakage, lifetime and leakage degradation in comparison with those of ordinary polycrystalline capacitors.

**Experiments and Results**

Sample preparation was carried out by ordinary RF sputtering onto single-crystalline SrTiO$_3$ substrates. The appropriate Ba/Sr ratio was determined to optimize the lattice constant mismatch between BSTO and SRO bottom electrodes. Prior to this, the effects of the lattice deformation on the dielectric constant of BSTO was evaluated by means of the first-principles computational simulations taking account of both energies of the lattice system and the electron system$^2$. The obtained result indicated the appropriate in-plane stress and tetragonal distortion could yield much higher dielectric constants than observed in cubic BSTO in ordinary polycrystalline films (Fig.2). The dielectric constant obtained in an SRO/20-nm thick Ba$_{0.4}$Sr$_{0.6}$TiO$_3$/SRO capacitor was as
high as 920 and its effective SiO₂ thickness was 0.085 nm, which corresponds the capacitance of 26 fF in a planar capacitor with dimensions of 0.18 micron by 0.36 micron. The leakage current observed in these capacitors was lower than 3×10⁻⁸ A/cm² in applied voltage range of -1.8 V to +1.8 V and maintained low values at higher fields (Fig. 3).

Reliability-related phenomena such as TDDB and degradation were examined in these capacitors and compared to those in ordinary polycrystalline capacitors with Ru electrodes and BSTO/SRO capacitors with Pt top electrodes. The lifetimes of the heteroepitaxial all oxide capacitors as obtained from breakdown tests at various temperatures and stresses revealed to exceed the lifetimes of the other types of capacitors (Fig. 4-6).
In addition, the leakage degradation observed in the present epitaxial capacitors was slighter than that of other capacitors(Fig.7-9). We attribute the high reliability observed in these heteroepitaxial capacitors to cleanliness in the SRO/BSTO interfaces.

Discussion

First, we shall discuss why our epitaxial capacitors exhibit much higher dielectric constants than polycrystalline capacitors. As expected from the computational simulation, it is evident from the result of comparison between epitaxial capacitors and polycrystalline capacitors with identical dielectric thickness and identical capacitor constitution, the mismatch induced lattice deformation to an appropriate degree is quite effective to obtain higher dielectric constant of these BSTO thin film capacitors. Crystal structure of BSTO films in epitaxial capacitors described in this paper was determined by X-ray diffraction: it exhibits tetragonal structure and has c axis of 0.404nm and a axis of 0.3905 nm. This is markedly contrasted to that the structure of conventional polycrystalline BSTO film is cubic. As well as the lattice deformation, our results indicated the importance of clean interfaces between BSTO and electrodes. To evaluate the differences between conductive oxide electrodes and metal electrodes, we fabricated SRO/BSTO/SRO and Pt/BSTO/SRO capacitors with identical bottom electrodes and BSTO films. The dielectric constant of SRO/30-nm thick BSTO/SRO capacitors was 550 while Pt/30-nm thick BSTO/SRO capacitors exhibited dielectric constant of 480. In thinner capacitors, this difference is more markedly contrasted: dielectric constant of 744 for SRO/20-nm thick BSTO/SRO capacitors and 338 for Pt/20-nm thick BSTO/SRO capacitors were obtained. These differences in dielectric constant might imply the existence of a low dielectric constant layer between BSTO and metal electrodes.
As well as extremely high dielectric constant, low leakage current even in very thin capacitors is also a distinctive characteristic in epitaxial capacitors. Though dominant factors governing leakage current of these thin film capacitors have not yet been clarified, we can point out some features of the epitaxial capacitors which are expected to yield lower leakage, such as smooth morphology and fewer ionic defects in heteroepitaxial interface between BSTO and SRO. The same features are also responsible for the high reliability of epitaxial capacitors.

The accumulation of oxygen defects at the boundary between ferroelectrics and electrodes is considered as one of the origins of fatigue and/or imprint phenomena in ferroelectric thin film capacitors. This kind of defect accumulation may cause interfacial electronic states at the electrode/BSTO interface in dielectric capacitors for DRAM applications and the consequent leakage degradation may cause further defect generation and will result in a dielectric breakdown. The BSTO/SRO heteroepitaxial interface may have fewer oxygen defects than metal/BSTO interface. In addition, oxide electrodes have been reported to act as oxygen defect sinks\(^3\), and the accumulation of oxygen defects after application of a unipolar stress will thus be less than that in the case of metal electrodes. Furthermore, in Ru electrode capacitors, degradation also seems to have their origin at anode interface. We speculate this kind of leakage degradation is attributed to oxygen defect generation at anode interface. On the other hand, in the case of SRO electrode, this anode degradation is also markedly reduced. This might indicate the oxide electrodes play the role of an oxygen reservoir(Fig.10). The comparison of our results shown in

Fig.7. Leakage degradation in epitaxial SRO/BSTO(30-nm thick)/SRO capacitor : I-V characteristics were measured after gate+3 V DC stress at 553 K for 100 to 1600 seconds.

Fig.8. Leakage degradation in polycrystalline Ru/BSTO(40-nm thick)/Ru capacitor.

Fig.9 Leakage degradation in Pt/BSTO(30-nm thick)/SRO epitaxial capacitor.
SUMMARY

We have observed a high capacitance of 0.085nm SiO₂ equivalent thickness, very low leakage current and high reliability in our developed SRO/BSTO/SRO heteroepitaxial capacitors, where oxide electrodes played important role to increase degradation resistance.

REFERENCES

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AN IMPORTANT FAILURE MECHANISM IN MOCVD (Ba,Sr)TiO$_3$ THIN FILMS: RESISTANCE DEGRADATION


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ABSTRACT

We have investigated the intrinsic resistance degradation behavior of fiber-textured MOCVD (Ba,Sr)TiO$_3$ thin films appropriate for use in advanced DRAMs and integrated decoupling capacitors, as a function of applied voltage polarity, thickness, temperature, and dc bias/field. The results suggest that there is a significant stoichiometry effect on the measured resistance degradation lifetimes. The measured degradation lifetime increases as the Ti content is increased from 51.0 to 52.0 at%Ti, and then decreases with higher at%Ti. Predicted resistance degradation lifetimes obtained from both temperature and voltage extrapolations to DRAM operating conditions of 85°C and 1.6 V exceed the current benchmark of 10 years for all of the films studied.

INTRODUCTION

The capacitance and leakage requirements placed on (Ba,Sr)TiO$_3$ (BST) films targeted for DRAM and integrated capacitor applications have led researchers to work primarily on achieving the optimum parameters for these properties. However, in addition to these, lifetime and reliability are also extremely important issues in the practical use of the capacitors. Therefore, it is crucial to determine failure mechanisms and estimate lifetimes based on analysis of these mechanisms.

The current benchmark for advanced DRAMs is a 10 year lifetime at 85°C and 1.6 V. Under these projected operating conditions, the most important failure mechanism in perovskite titanate thin films is likely to be resistance degradation, which is defined as a slow increase of the leakage current under a constant applied electric field after prolonged times. This is a critical issue in practical memory applications of these films since it may cause a change in the stored charge or charge retention ability, due to an increase in leakage current during long term memory operation.

There have been only a few reports about the resistance degradation behavior of BST thin films appropriate for DRAM applications, and none of them included a comprehensive study of external and material parameter effects on resistance degradation [1-3]. Also, no optimization has been performed to improve on the resistance degradation lifetime of such films; however, significant impact can be expected from proper control of stoichiometry and/or doping, as well as of processing. This is an area that will need much attention as BST technology moves closer to production.

In this paper, the intrinsic resistance degradation behavior of fiber-textured MOCVD BST thin films appropriate for advanced DRAMs is analyzed as a function of applied voltage polarity, dc bias/field, temperature, film thickness, and the (Ba+Sr)/Ti (A:B) ratio. Because lifetimes for these samples under projected operating conditions are expected to be prohibitively long, judicious choice of accelerated testing conditions for both temperature and voltage/field and appropriate extrapolation techniques are necessary [4]. The estimated lifetimes using appropriate extrapolation methods under the projected DRAM operation conditions will be discussed.

EXPERIMENTAL PROCEDURES

Pt bottom electrodes were deposited onto 6-inch wafers by electron-beam evaporation, directly onto SiO$_2$/Si at 315°C, to a thickness of 100 nm [5]. X-ray diffraction revealed that the Pt films were strongly [111] oriented. BST films were then deposited on the Pt-coated Si wafers by a liquid-delivery-source chemical vapor deposition technique at approximately 640°C, to thicknesses ranging from 24 to 160 nm [6]. The Ba-to-Sr ratio was chosen to be 70/30, while the (Ba+Sr)/Ti (A:B) ratio was varied from 49/51 to 47/53. The film compositions and thicknesses were determined by wavelength dispersive x-ray fluorescence spectroscopy [6]. Transmission electron microscopy and x-ray diffraction revealed that the BST films had a columnar microstructure and were strongly [100] textured, with minor [110]- and [111]-oriented components, depending on film thickness. Pt top electrodes were evaporated onto the BST through a shadow mask so as to define capacitors for electrical testing, again at a substrate temperature of 315°C [5].

DC leakage currents were measured between room temperature and 250°C using a Keithley 617 programmable electrometer with a built-in voltage source. Care was taken to discriminate the true leakage from relaxation currents [7].

In this study, the characteristic measured degradation lifetime value, $t_d$, is defined as the time at which current across the sample increases by one order of magnitude above its minimum value before the start of degradation, $t_s$ (Fig. 1).

RESULTS AND DISCUSSION

Voltage Polarity Dependence

Figure 2 shows the polarity dependence of the resistance degradation behavior of a 40 nm, 53.3 at%Ti BST sample at 225°C under a constant dc electric field of 875 kV/cm. As can be seen, there is almost no polarity dependence (between stressing the top electrode at positive and negative dc biases), suggesting that it is an intrinsic effect. Extrinsic effects, such as the moisture related early degradation observed for PZT films, which causes a severely polarity-dependent degradation rate, would make the resistance degradation analyses difficult [8,9]. Numata et al. also observed a severe polarity-dependent resistance degradation for sputtered BST films [1]. Given this polarity-independent degradation behavior, it is also likely that the defects causing the degradation are distributed homogeneously across the film thickness.

![Figure 1: Definition of characteristic resistance degradation lifetime ($t_d$).](image1)

![Figure 2: Voltage polarity dependence of resistance degradation.](image2)