Heteroepitaxy on Silicon
MATERIALS RESEARCH SOCIETY SYMPOSIA PROCEEDINGS

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MATERIALS RESEARCH SOCIETY SYMPOSIA PROCEEDINGS


Heteroepitaxy on Silicon

Symposium held April 16–18, 1986, Palo Alto, California, U.S.A.

EDITORS:

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Kopin Corporation, Taunton, Massachusetts, U.S.A.

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*Invited paper
Preface

This volume contains papers presented at the symposium on “Heteroepitaxy on Silicon” held in Palo Alto, California, April 16-18, 1986. The symposium was the first of its kind devoted to the subject of heteroepitaxy on Si. Silicon homoepitaxy is well established and is vital in the Si industry. If heteroepitaxy on Si is successful, the applications will be considerable, ranging from optical communication, high-speed integrated circuits, to solar cells. Understanding and controlling the crystal growth processes present a major challenge to material scientists. Significant advances in heteroepitaxy and device fabrication have recently been achieved by many workers.

The symposium was well attended (over two hundred attendees) and represented an international forum for this emerging subject. Progress is outstanding, both in terms of fundamental understanding and in the area of practical applications. Over thirty papers were presented in oral sessions, and the majority of these are incorporated in this book.

Nine internationally recognized scientists were invited to give papers on topics, ranging from material and device properties of GaAs on Si, initial nucleation phenomena and the growth of insulators and metals on Si. An evening panel session on “Future of GaAs on Si” brought out lively discussion. The issues and responses from the panelists have been tabulated and described in the volume.

Symposium Co-Chairmen

John C. C. Fan    John M. Poate

July 1986
Acknowledgments

We wish to thank all the contributors and participants who made the symposium so successful. We particularly would like to acknowledge the invited speakers, who provided excellent summaries of specific areas and set the tone of the meeting. They are:

M. Akiyama  S. Sakai
H. Ishiwara  R. T. Tung
H. Kroemer  K. L. Wang
H. Morkoc  T. H. Windhorn
Y. Ohmachi

We are also grateful to the panelists who helped bring out many important issues on "GaAs on Si". They are:

M. Akiyama  R. Koyama
J. Goodman  H. Kroemer
H. Kim  H. Morkoc

We are deeply indebted to the session chairs who directed the sessions, guided the discussions, and gave invaluable help in getting the papers refereed. They are:

J. C. C. Fan  J. M. Poate
R. P. Gale  G. A. Rozgonyi
J. S. Harris  B.-Y. Tsaur
H. Ishiwara  S. Wang
J. M. Phillips

Special thanks are also due to Ms. Henrietta Weston and Ms. Cami Davis. It is through their efforts that the symposium and the book have come to fruition. We would like to thank Ms. Karen Martelli for her support in running the evening panel session.

It is our great pleasure to acknowledge with gratitude, the financial support provided by the Air Force Office of Scientific Research (Dr. Kevin J. Malloy and Dr. Gerald L. Witt).
Report of Panel Session (April 17, 1986)

Future of GaAs on Si

Moderator: John C. C. Fan, Kopin Corporation, Taunton, MA

Panel Members:

M. Akiyama  OKI Electric
J. Goodman  Stanford University
H. Kim  Ford Microelectronics
R. Koyama  TriQuint Semiconductor
H. Kroemer  Univ. of California, Santa Barbara
H. Morkoc  University of Illinois

There are a number of critical issues facing GaAs on Si technology. The panel session consisted of leaders in the GaAs on Si community. Their viewpoints, shown in tabulated form, were presented for general discussion in the session which was attended by about 200 people. There is considerable excitement on the rapid progress in this technology, and all its potential applications. Major technological advances are still required before this technology will be successful.
## Question 1  What are the potential applications of GaAs on Si in order of importance?

<table>
<thead>
<tr>
<th>Akiyama</th>
<th>Goodman</th>
<th>Kim</th>
<th>Kroemer</th>
<th>Koyama</th>
<th>Morkoc</th>
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<tbody>
<tr>
<td>ICs with GaAs and Si Devices</td>
<td>Optical Interconnects</td>
<td>Discrete and Small Scale Integrated Circuits</td>
<td>Optoelectronic Integration</td>
<td>HEMT/Si ICs</td>
<td>Replace GaAs Substrates</td>
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<td>GaAs power devices</td>
<td>Mono-lithic Microwave Substrates</td>
<td>Power FETs (microwave)</td>
<td>GaAs/AlGaAs ICs</td>
<td>Heterojunction Bipolar Transistor/Si ICs</td>
<td>Hybrid Devices for Optical Detectors and Displays</td>
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<td>Solar Cells</td>
<td>Multifunction Si-GaAs digital circuits</td>
<td>Digital Integrated Circuit and Mono-lithic Microwave Integrated Circuit</td>
<td>Power FETs</td>
<td>GaAs/CMOS Si ICs</td>
<td>Integrated GaAs and Si devices</td>
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<td>Solar Cells</td>
<td>Optical Integration</td>
<td>Solar Cells</td>
<td>III-V Electro-Optic/Si ICs</td>
<td>Optoelectronics in Si</td>
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</table>
Question 2  What are the major material problems facing GaAs on Si, in order of importance?

<table>
<thead>
<tr>
<th>Akiyama</th>
<th>Goodman</th>
<th>Kim</th>
<th>Kroemer</th>
<th>Koyama</th>
<th>Morkoc</th>
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<tbody>
<tr>
<td>Tensile stress (wafer bending, cracking)</td>
<td>Achieve low dislocations (&lt;10^3 cm^-2)</td>
<td>Low dislocation density and antiphase domain</td>
<td>Threading Dislocations</td>
<td>Dislocation/Defects/ Impurities</td>
<td>Materials quality relating to dislocation and strain caused by thermal mismatch</td>
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<td>Defects which are not indicated by etch pit densities</td>
<td>Obtain good uniformity</td>
<td>Reproducible low-dislocation growth</td>
<td>Cross-doping</td>
<td>Stress in the interface and in bulk epi</td>
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<tr>
<td>Demonstration of high-quality optical devices and ICs</td>
<td>Minimize strain</td>
<td>Semi-Insulating epi</td>
<td>Anti-Phase Domain</td>
<td>Uniformity/Reproducibility of the epi layers</td>
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<td></td>
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<td></td>
<td>Produce 4&quot; or larger wafers</td>
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<td></td>
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<td>Cost of epi</td>
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Scaling up to 6", 8"
Question 3 What are the proposed solutions for these materials problems?

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<tr>
<th>Akiyama</th>
<th>Goodman</th>
<th>Kim</th>
<th>Kroemer</th>
<th>Koyama</th>
<th>Morkoc</th>
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<tbody>
<tr>
<td>Clarify growth mechanism and relationship between growth and crystallization</td>
<td>Selective and/or embedded growth</td>
<td>Low dislocation solid phase regrowth, super lattice buffer</td>
<td>Intense production scale-up development</td>
<td>Strained Layer Superlattices</td>
<td>Gain Experience</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>(211)</td>
<td>Use dislocation control techniques and high-quality materials</td>
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<tr>
<td>Accumulate materials and device data on the material</td>
<td>Strain-low growth temperature (plasma-enhance MOCVD)</td>
<td>R&amp;D in growth kinetics for the growth systems</td>
<td></td>
<td>Either (211) or high temperature anneal on (100)</td>
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<td></td>
<td>TLC</td>
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</table>
**Question 4** What are the device processing problems facing GaAs on Si, in order of importance?

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<tr>
<th>Akiyama</th>
<th>Goodman</th>
<th>Kim</th>
<th>Kroemer</th>
<th>Koyama</th>
<th>Morkoc</th>
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<tr>
<td>Wafer bending</td>
<td>Maintenance of circuits during GaAs growth/device processing</td>
<td>Inherent step height problem during GaAs and Si devices</td>
<td>Built-in strain during cool down</td>
<td>Wafer flatness (&lt; few um)</td>
<td>In all aspects GaAs on Si makes processing simpler</td>
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<td>Adaptation of processing chemistry, thermal treatment compatibility</td>
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<td>Equipment compatibility (handling), warping, wafer detection system etc.</td>
<td>Cleavage incompatibility</td>
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<td>For optical interconnects overcome basic incompatibility of optical and electronic material requirements</td>
<td>Adoption/conversion of large 8&quot; Si line into GaAs line</td>
<td>Possible incompatibility with MOS</td>
<td>Uniformity and reproducibility</td>
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Cambridge University Press 978-1-107-41119-7 - Heteroepitaxy on Silicon Edited by J. C. C. Fan and J. M. Poate Frontmatter More information
<table>
<thead>
<tr>
<th>Question 5: Is GaAs on Si technology really needed? If so, when will it be commercially available?</th>
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<tbody>
<tr>
<td>Akiyama</td>
</tr>
<tr>
<td>Yes, GaAs/Si has many advantages (such as high thermal conductivity, larger wafer sizes, light weight, etc.)</td>
</tr>
<tr>
<td>Reasons: Low cost nearly competitive with Si epi</td>
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<td>1987-1988</td>
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