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978-1-107-12701-2 — Robust Design of Digital Circuits on Foil
Kris Myny , Jan Genoe , Wim Dehaene
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Robust Design of Digital Circuits on Foil

Covering both TFT technologies and the theory and practice of circuit design, this book equips engineers with the technical knowledge and hands-on skills needed to make circuits on foil with organic or metal-oxide based TFTs for applications such as flexible displays and RFID.

It provides readers with a solid theoretical background and gives an overview of current TFT technologies including device architecture, typical parameters, and a theoretical framework for comparing different logical families. Concrete, real-world design cases, such as RFID circuits and organic and metal-oxide TFT-based 8-bit microprocessors, enable readers to grasp the practical potential of these design techniques and how they can be applied.

This is an essential guide for students and professionals who need to make better transistors on foil.

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The ideal engineer is a composite. … He is not a scientist, he is not a mathematician, he is not a sociologist or a writer; but he may use the knowledge and techniques of any or all of these disciplines in solving engineering problems.

N. W. Dougherty, 1955

A design is what a designer has when time and money run out.

James Poole, chief architect for Disneyland

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Preface

Guided Tour

This book is the result of several years of electronics engineering research that was performed in close cooperation between technologists and circuit design experts. The target of the research was to bring maturing thin-film transistor (TFT) technologies to a level where real, relevant circuits can be made. Relevant in this context means scientifically relevant as well as economically feasible. To enable this, types of circuit techniques were used. The advantage of the cross-level research, however, is that it is not limited to circuit techniques alone. Also technology improvements and extensions were conceived and tested. In this way dual gate TFTs were put on the map, for example.

To achieve the mission described we originally tackled several design cases. The purpose of this was to make sure that the research really produced the key enablers to enable concrete actual design. However, that is not how we present it here. Once the results were established, it seemed more logical and technically profound to present the state of the art the other way. Otherwise said: The order in which to look for things is not necessarily the best order to present those things. Therefore, the book evolved from more theoretical background information to concrete design cases.

The book starts with an introductory chapter situating TFT transistors in their application domain. It also situates organic and metal-oxide TFTs on foil next to the other TFT technologies. Organic and metal-oxide TFT are the technologies that are used in the subsequent chapters when TFT based circuits are discussed from a digital design perspective. The introductory chapter does not strive for historical completeness. It only gives a high level overview of the different TFT technologies that are available and their (potential) field of application. Details can eventually be found in the many references in the chapter.

After the introduction the book falls into two major parts. The first part, Chapters 2 to 4, discusses the necessary background for digital circuit design with TFTs on foil. The discussion first addresses the different devices that are used in Chapter 3. The different device architectures are described and typical parameters are given. These devices are further used to design logical gates in Chapter 3. Different logical families are compared to each other in terms of energy, area, robustness, and performance. For this we use a theoretical framework that is very similar to the framework that is classically used to analyze silicon CMOS gates. Chapter 4 adds the influence of technological variability on these gates to the picture. It should be mentioned that this is work in progress. Much more, mainly experimental work, to quantify TFT on foil variability is required. In general terms it can be stated that the relatively classical variability models are most likely to be a good starting point, yet further calibration with experimental data is required. Eventually the models will have to be refined.

The last part of the book contains the most important design cases that were used during the research. Chapter 5 discusses the RFID circuits that were designed, processed, and tested. In Chapter 6 the first organic, and later metal-oxide, TFT based 8-bit microprocessors are discussed. The discussion of these circuits is interesting for the circuits as such, as they are finding their way to wider application already. Of course, the design techniques in this book can be much more widely applied than for RFID or microprocessors alone.

Glancing at the Horizon

Of course, research is never complete and never ends. Each solved research question usually opens a few new ones. It is not different in this case. It is shown in this book that circuits on foil with organic or metal-oxide based TFTs are feasible. The influence of device physics related parameters has been mapped. However, it is not yet clear where the fundamental technological limitations are situated. For that more research – and perhaps a new book – is required. This future research should be centered on the following fundamental questions: The first question is which technological improvements are needed and can be realized to further improve the intrinsic quality of the devices. Can the mobility be further enhanced? How about capacitance? Can we reduce the overlap capacitance by making the devices self-aligned? At the time of this writing this is under way. Is it possible to have complementary devices? Having p and n devices of equal or at least comparable current capability would definitely further boost the performance versus energy trade-off of the TFT based circuits.

A next group of research questions is centered on modeling. There is definitely a need for more accurate, preferably device physics based, compact models for the TFTs. This includes modeling of long- and short-range variability. Long-range variability especially needs to be further analyzed as it will be a typical design issue in large area electronics. Numerical or physical models that are accurate will be a key factor to better performing circuits with a higher yield.

Last but not least there is the question of future scaling. How about next generation TFT technologies and circuits? What is the road map for these technologies? Will there be a Moore's law for circuits on foil?

The preceding questions are not answered in this book. However, the basic information to start designing circuits on foil and eventually take the research a step further is provided. If you are technologists working in circuits on foil and you want to see how this technology can be used, this book is the place to start. The same is true if you are a circuit designer and you want to figure out what the properties of TFT on foil devices are and how to put them together effectively in digital circuits.

List of Symbols and Abbreviations

Symbol	Description	Unit
ΔL	Channel length of the pinched off region	μm
ΔV	Overshoot on the output node	V
α_1, α_2	Correction factors for the channel capacitance	
β	Current factor of the I_{DS} equation	nF/Vs
γ	Proportionality or technology factor	
ε_0	Vacuum permittivity (8.854187817)	pF/m
ε_r	Relative permittivity	
$\sigma(V_T), \sigma(\mu), \sigma(I_{on})$	Standard deviation of V_T, μ, I_{on}	
ξ	Sensitivity of the back gate	
λ	channel length modulation factor	1/V
μ and $\overline{\mu}$	Mobility and average of mobility	cm^2/Vs
A_{gd}, A_{gs}	Area of the gate-drain and gate-source capacitance	μm^2
A_{gsc}	Area of the gate-to-drain channel and gate-to-source channel capacitance	μm^2
A_μ	Area proportionality constant of μ	%μm
A_{V_M}	(Small signal) gain at V_M	
A_{V_T}	Area proportionality constant of V_T	Vμm
C	Capacitance	F
C_{ch}	Channel capacitance	F
C_{ext}, C_{int}	Extrinsic and intrinsic capacitance	F
C_g	Input gate capacitance	F
C_{gcdx}, C_{gcsx}	Gate-to-drain and gate-to-source channel capacitance of transistor x	F
C_{gd}, C_{gs}	Gate-drain and gate-source capacitance	F
C_{gdox}, C_{gsox}	Gate-drain and gate-source overlap capacitance of transistor x	F
C_{gx}	Gate capacitance of transistor x	F
C_{iref}	Capacitance of the minimum sized inverter	F
C_L	Load capacitance	F
D_x	Spacing between two transistors	μm
F	Overall effective fan-out	

Symbol	Description	Unit
FW	Finger width of source and drain contacts	µm
GND	Signal ground	
H	Electromagnetic field	A/m
I_D	Current through a diode	A
I_D, I_G, I_S	Current at the drain, gate and source of a transistor	A
I_{DS}	Drain-source current $(I_D-I_S)/2$	A
$I_{DS,lin}$, $I_{DS,sat}$	Drain-source current of a transistor operated in linear or saturation regime	A
I_{on}	On-state current of a transistor	A
I_{PD}, I_{PU}	Pull-down and pull-up current	A
J	Current density	A/cm^2
L	(1) Transistor's channel length (2) Inductance	µm H
L_{eff}	Effective channel length	µm
N	Chain of N inverters	
N_{opt}	Optimal number of inverter stages	
OPS	Operations per second	OPS
R	(1) Resistance (2) Radius reader antenna	Ω cm
$R_{eq\ l}$, $R_{eq\ d}$	Equivalent resistor of the load and drive transistor	Ω
$R_{on,\ TD}$, $R_{on,\ TL}$	On-resistance of the drive and load transistor	Ω
R_{ref}	Resistance of the minimum sized inverter	Ω
S	Sizing factor	
S_{V_T}	Distance proportionality constant	V/µm
$V_{BG,D,G,S}$	Potential of the back-gate, drain, gate, and source node, respectively	V
V_D	Voltage across a diode	V
VDD	Supply voltage	V
V_M, V_{trip}	Trip point	V
V_T	Threshold voltage	V
$V_{T,0}$	Threshold voltage with 0 V source-back-gate bias	V
$V_{T,\ drive}$, $V_{T,\ load}$	Threshold voltage of the drive and load transistor	V
W	Transistor's channel width	µm
f	Effective fan-out	
f_{opt}	Optimum value for effective fan-out	
g_m	Transconductance	S
g_o	Output conductance	S
r	Transistor ratio	
r_o	Output resistance	Ω
t_{d0}	Intrinsic delay	s

Symbol	Description	Unit
t_{ox}	Thickness of the gate dielectric	m
t_p	Propagation delay	s
t_{pHL}, t_{pLH}	Propagation delay for a transition from high to low or low to high	s

Abbreviation	**Description**
2T1C	2-transistor-1-capacitor
3D	Three dimensional
4k2k	3840x2160 pixels
a-IGZO	Amorphous Indium-Gallium-Zinc-Oxide
a-Si	Amorphous Silicon
AC	Alternating current
ADC	Analog-to-digital converter
ADD	Addition
Al	Aluminum
Al_2O_3	Aluminum oxide
ALD	Atomic layer deposition
ALU	Arithmetic and logic unit
AM	Active matrix
AM LCD	Active-matrix liquid crystal display
AMOLED	Active-matrix organic light-emitting diode
Au	Gold
BCE	Back-channel etch
buf3	Buffer inverter, size is 3 times normal inverter
C-2C	Capacitor-double-capacitor architecture
CMOS	Complementary metal-oxide-semiconductor
Clk, CLK	Clock
D	Drain
D-flip-flop	Data or delay flip-flop
D2D	Die to die or inter die
DAC	Digital-to-analog converter
DC	Direct current
DC-DC	DC to DC converter
DEC	Decrement
ELA	Excimer laser annealing
EMI	Electromagnetic interference
EPC	Electronic Product Code
ES	Etch stopper
EXNOR	Exclusive NOR gate
F, FF, FS	Fast, fast-fast, and fast-slow corner

Symbol	Description	Unit
F'	Compensated fast corner	
FPGA	Field-programmable gate array	
G	Gate	
HF	High frequency	
IC	Integrated circuit	
INC	Increment	
ISO	International Organization for Standardization	
JMP	Jump	
LC	Resonant circuit, consisting of an inductor and a capacitor	
LCD	Liquid crystal display	
LD	Load	
LED	Light-emitting diode	
LSL, LSR	Logic shift left and right	
LTPS	Low-temperature polycrystalline silicon	
MC	Monte Carlo	
MEC	Maximum equal criterion	
MOSFET	Metal-oxide-semiconductor field-effect transistor	
MUX	Multiplexer	
n-TFT	N-type thin-film transistor	
NAND	Not-AND logic gate	
NOOP	No operation	
NOR	Not-OR logic gate	
OLED	Organic light-emitting diode	
opcode	Operational code	
OTFT	Organic thin-film transistor	
p-TFT	p-type thin-film transistor	
PC	Program counter	
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)	
PEN	Polyethylene naphthalate	
RC	Resistor-capacitor circuit	
RF	Radio frequency	
RFID	Radio-frequency identification	
RGB	Red Green Blue	
ROM	Read-only memory	
RR	Register select bits of the microprocessor	
RT	Room temperature	
S	Source	
S, SF, SS	Slow, slow-fast, and slow-slow corner	
S'	Compensated slow corner	

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Symbol	Description	Unit
Si	Silicon	
SiN_x	Silicon nitride	
SNM	Static noise margin	
SPC	Solid phase crystallization	
SUB	Subtract	
T, TT	Typical and typical-typical corner	
T_D, T_L	Drive and load transistor	
T_D, T_S	Drive and select transistor in a 2T1C pixel scheme	
TFT	Thin-film transistor	
Ti	Titanium	
UHF	Ultra-high frequency	
VHDL	Very-high-speed integrated circuits hardware description language	
VTC	Voltage transfer curve	
WID	Within die	
WORM	Write-once-read-many times	