1 Thin-Film Transistor Technologies on the Move? From Backplane Driver to Ubiquitous Circuit Enabler?

This chapter briefly describes the product requirements for active matrix display with a focus on the technology used for the backplanes of these displays. A short overview is given of the different device technologies that are used today to implement display backplanes. Next innovation in these technologies by means of organic and oxide based devices on foil is considered. Eventually this will lead to the realization of flexible displays.

In the second part of this chapter we broaden the view. Flexible electronics foil has more applications than displays alone. Other large area electronic systems are envisaged; low-cost RFID, small controllers, and so on, can also be envisaged.

1.1 Backplanes for Active Matrix Displays

Thin-film transistors are omnipresent in our daily lives, mostly as a backplane technology for displays. The rapidly growing display industry is continuously increasing the demand for better performing thin-film transistors to be integrated in next generation display panels. The panel sizes are not limited to larger backplanes for television applications alone, but also to smaller backplanes for mobile devices such as smart phones and tablets.

One tendency in this application field is steady improvement of the displayed image quality, such that the appearance of images becomes much sharper for every new product generation. The current standard for televisions is known as *high definition* and comprises a backplane array of 1920 × 1080 pixels. The next standard is defined as *ultra-high definition,* or *4k2k*, with an array size of 3840 × 2160 pixels. High-end panels in the mobile phone industry continuously squeeze in more and more pixels per inch, resulting in an ultra-sharp, non-pixelated image appearance at typical viewing distance. Current state-of-the-art smart phones exhibit a pixel density above 300 pixels per inch. The resolution of the smart phone displays increases but the size of the display remains unaltered because it is dictated by the size of the phone itself. This demands smaller pixels and better performing thin-film transistors. Another important tendency in display research is the reduction in power consumption to realize green electronics and to save battery life for handheld devices. Also in this case, better performing thin-film transistor backplanes are required to reduce the display's power consumption.

Displays in televisions and handheld devices are active-matrix (AM) displays consisting of a transistor backplane actively driving a front plane. Liquid crystal (LC) is the front plane technology that is mostly used in current televisions. An alternative front plane is based on organic light-emitting diodes, or OLEDs, recently introduced in handheld devices on the market. The advantage of OLED based displays is that the front plane directly emits light. LC based front planes actually selectively block the light from a backlight. Therefore, OLED based displays usually have better contrast and are more energy efficient. An OLED is a current driven device that emits light, whereby a change in current through the OLED results in different brightness values for the OLED. This front plane technology thus requires a high current-drive compared to LCD and is more demanding for the transistor backplane.

At the current state of the art, the substrate used for the display backplanes in production is glass. The glass size – determining the number of displays per substrate – is currently at generation 10, which has a huge physical size of 2880 × 3130 mm^2. Next generation applications are focusing on lightweight devices, requiring ultra-slim glass plates or plastic foil to be used as substrate. Displays fabricated on plastic substrates are very appealing for future devices, because of the possibility of realizing unbreakable, flexible, or rollable displays. This will be discussed in a later paragraph.

1.1.1 Amorphous Silicon

The most widely used thin-film transistor technology for backplanes employs amorphous silicon, or a-Si, as a semiconductor [1]. The fabrication process of an a-Si transistor backplane requires only 4–5 photo masks, and it results in n-type only devices. The standard process temperature for the semiconductor is about 250°C; the maximum temperature used in the process flow is 350°C for the SiN_x gate dielectric [2]. a-Si backplanes exhibit very good uniformity, which is due to the amorphous nature of the semiconductor with an average carrier mobility between 0.5 and 1 cm^2/Vs. This mobility value is sufficient for current generation displays, but might be at the limit for next generation high-end devices where the required resolution and current drive increase. As a result of the key merits of a-Si transistor backplanes, which are technology maturity, good uniformity, and low fabrication cost, they are still predominantly used for the current and near-future LC based displays.

Despite their wide use, a-Si transistors suffer from continuous bias instabilities resulting in threshold voltage shifts over time [3]–[5]. Current LC based displays can accommodate these shifts. However, in combination with the more stringent requirements OLED based technologies pose for backplane devices, threshold shifts will become prohibitive. A threshold voltage shift introduces a variation of the source-drain current of the a-Si transistor, which directly translates into non-uniform light emission in OLED displays. Compensating for this will lead to more complex pixel circuits [6]–[9]. The need to design multiple transistors per

pixel will finally limit the minimum pixel size (combined with the low charge carrier mobility) and therefore the final display resolution [10]. A more stable transistor technology than a-Si will thus be required in the near-future if the evolution in display resolution is to be sustained.

1.1.2 Low-Temperature Polycrystalline Silicon

Low-temperature polycrystalline silicon (LTPS) thin-film transistors are an alternative backplane technology to realize current and next generation AMLCD or AMOLED displays. LTPS transistors can be fabricated by multiple methods, among others excimer laser annealing (ELA) and solid phase crystallization (SPC) [11]–[14]. ELA LTPS transistors can exhibit a mobility exceeding 100 cm^2/Vs as a result of the crystallinity of the semiconductor. ELA also allows fabrication of both p-type and n-type transistors. LTPS backplanes are currently being manufactured for high-end displays given the enhanced mobility compared to a-Si transistors and the process temperature, which is still within the budget of glass substrates.

LTPS technology is also a viable candidate to fulfill next generation display requirements, such as reduced power consumption and faster switching backplanes. Moreover, the availability of a complementary (p-type and n-type) technology paves the way to integrate the peripheral display driver circuit directly on the display backplane, resulting in reduced wire fan-out [15]. Some drawbacks for this technology compared to a-Si are the higher process temperature, the device-to-device non-uniformity, and the higher cost and lower yield caused by a more complex process flow with additional mask steps [16]. This increased cost of the backplane technology is partly compensated by a reduced system cost due to the integration of the peripheral display driver circuit. The device non-uniformity stems from the presence of grain boundaries and the limited laser exposure area in one shot [13]. As a result, the pixel engine for AMOLED displays will be more complex than a traditional 2-transistor 1-capacitor (2T1C) circuit in order to compensate for V_T-mismatch in the panel area [6], [17], [18]. This is nevertheless acceptable as the footprint of the transistor can be much reduced compared to a-Si TFT, as a consequence of the better intrinsic performance. This allows integrating more complex pixel engines that can compensate for even more issues than V_T non-uniformities, for example, OLED degradation.

1.1.3 Organic Thin-Film Transistors

Research on organic thin-film transistors became very appealing as a result of the foil-compatible process temperature for these semiconductors combined with a performance similar to a-Si TFTs [19]. At the current state of the art, organic thin-film transistors are even outperforming a-Si TFTs with carrier mobility up to 10 cm^2/Vs [20]–[24]. Therefore, organic TFTs is another viable candidate for next generation display technologies, especially on flexible substrates. Moreover, the processing techniques are not limited to expensive high-vacuum coating; solution

casting [20]–[23]; low-vacuum deposition [25], [26]; and even deposition at atmospheric pressure [27] are also possible. The applicability of solution-processing organic materials opens the perspectives of a new application field focusing on low-cost printed and flexible electronics. Gelinck et al. have demonstrated integrated circuits fabricated by polymer layers only, even for the contacts [28]. Also, printed transistors and circuits have been demonstrated [29]–[31]. It should be said that printed technology at the current state of the art suffers from excessively high device variability. Most organic transistors are p-type transistors. Recently, n-type TFTs have been explored to match with p-TFTs for complementary technology applications. The main disadvantages of organic thin-film transistor technologies are lack of environmental and bias stability. However, recent developments show major improvements for these instabilities [22], [24]. Finally, organic semiconductors tend to form polycrystalline layers with randomly distributed grain boundaries resulting in larger device non-uniformities compared to a-Si TFTs. The bias instabilities and non-uniformities also imply the need for more complex pixel compensating circuits for AMOLED displays [32]–[34]. This will ultimately limit the resolution of the displays that can be designed with organic TFT based backplanes.

1.1.4 Metal-Oxide Thin-Film Transistors

The field of metal-oxide thin-film transistors gained worldwide interest after the report of Nomura et al. about a single-crystalline metal-oxide semiconductor yielding great performance (carrier mobility of 80 cm^2/Vs), which truly demonstrated the potential of this type of semiconductor [35]. In the subsequent year, the same group fabricated amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs on flexible substrates resulting in large mobility compared to a-Si TFTs: up to 9 cm^2/Vs [36]. Because of the potential low process temperature, the usage of conventional deposition techniques, and the promising transistor performance [1], [37], [38], metal-oxide TFTs are undoubtedly candidates for next generation display technologies and are currently already present as backplane in today's consumer products. Jeong et al. [39] reported recently on the threshold voltage uniformity of a-IGZO TFTs, exhibiting a standard deviation of 0.1 V for long-range uniformity and 0.01 V for short-range uniformity. This is much better than the 0.1 V standard deviation for short-range uniformity in ELA TFTs. This is classically attributed to the amorphous nature of the oxide in the TFTs. As a consequence, a simple 2T1C pixel engine for AMOLED displays will be sufficient. Also the line driver can be integrated [39].

Line drivers in metal-oxide TFT technology are much better candidates for integration on the backplane. The higher performance of oxide technology results in faster circuits necessary to achieve the frame rates and smaller peripheral IC size. All of this sounds like a success story; however, the downside of the medal for this semiconductor is the bias instability [37], [38]. This instability may result in more complex pixel engines, after all, which will require more area compared to simple 2T1C pixel engines. Moreover, complementary circuits are not feasible in

Table 1.1. Overview of different TFT technology options with their properties

TFT technology	Amorphous silicon	Low-temperature polycrystalline silicon	Organic	Amorphous metal-oxide
Charge carrier mobility [cm^2/Vs]	0.5–1	~30–100	0.1–10	5–50
Device uniformity	Good	Poor	Poor	Good
AMOLED pixel engine	Complex	Complex	Complex	Simple / complex
Bias stability	Poor	Good	Poor	Under evaluation
Process temperature	250°C 350°C (SiN_x)	~500°C	RT	RT – 350°C
Semiconductor	n-type	CMOS	p-type n-type possible	n-type
Mask steps	4–5	6–9	4–5	4–5
Cost	Low	High	Low	Low

the current state of the art, since the performance of p-type oxide semiconductors is still very limited compared to that of n-TFTs. The availability of a complementary technology would be beneficial for robustness, speed, and power of the peripheral IC, which then would not be limited to a line driver only. As a final note, very recently, metal-oxide thin-film transistors and circuits have been demonstrated by means of solution-processing at room temperature, which potentially removes vacuum steps in the manufacturing flow [40].

1.1.5 Current TFT Technology Overview

Table 1.1 lists the properties of the previously discussed TFT technologies. Even though a-Si TFTs are the most widespread technology in production for present-day backplanes, their low charge carrier mobility will be insufficient to comply with next generation display standards. These future displays require low-power operation, exhibit ever-increasing panel resolutions, and will most likely introduce AMOLED as a front plane technology. AMOLED demands more and more precise current from the backplane technology. All these requirements lead to the need for better performing backplane technologies. LTPS and amorphous metal-oxide TFTs are the most promising candidates. Key advantages for LTPS backplanes are the intrinsically higher performance and the potential to integrate p-type and n-type TFTs simultaneously. This advantage allows integrating a complex peripheral circuit that reduces the overall system cost. Also amorphous metal-oxide TFTs exhibit improved charge carrier mobility compared to a-Si TFTs. Moreover, metal-oxide semiconductors can be deposited using conventional tools, enabling fast integration in current a-Si fabs. Metal-oxide backplanes can be fabricated with a larger

yield compared to LTPS because of a less complex process flow and the possibility of using a simple pixel engine. All these merits for metal-oxides may lead to the use of this technology for future display panels, in spite of the availability of LTPS TFTs in today's high-end products. Finally, we should remark that a hybrid technology with n-type metal-oxide transistors and p-type organic transistors can be envisaged in the future to combine the best of both worlds.

1.1.6 Options for Flexible Displays

Unbreakable, flexible, and even rollable displays are attractive options for integration of displays in all sorts of future applications. Envisage a rollable tablet computer, for example. Rollable displays imply the necessity to replace the rigid glass substrate by a flexible substrate such as ultra-thin glass, stainless steel foil, or plastic foil. In this section, the following technological solutions resulting in flexible TFT backplanes will be briefly discussed:

- Transfer to foil,
- Direct processing on high-temperature foil,
- Direct processing on low-temperature foil.

The first option, transfer to foil, does not require low process temperatures during backplane fabrication and is therefore mostly beneficial for silicon TFT technologies [41], [42]. At the end of the fabrication flow, the stack on foil is removed by laser debonding from the temporary carrier. After the AM LCD panels, AMOLED displays and even an 8-bit microprocessor have already been demonstrated by this method [43]–[45].

The other two options require matching of the maximum process temperatures to the temperature budget of the foil. There are several substrate options available: metal foils (such as stainless steel foil) or polymer substrates. Table 1.1 suggests that organic and amorphous metal-oxide TFTs may offer proper matching of process temperature budgets to high-temperature foils and even to low-temperature foils (e.g., <180°C for polyethylene naphthalate (PEN) foil), without severe impact on the device performance [1], [19], [37], [38], [46]. Noda et al. demonstrated in 2010 the first rollable AMOLED display based on organic TFTs [47]. Finally, substrates made of paper or even banknotes are within the possibilities for organic and metal-oxide TFTs, opening perspectives for new potential application fields [48]–[51].

High-temperature foils allow the highest temperature to be maintained in the process flow. This occurs when SiN_x is processed as gate dielectric (350°C). Stainless steel foil has been explored for a-Si TFTs [52] and is considered as an option for LTPS TFTs [53]. Stainless steel foil, however, does not give a solution for fully transparent displays. For this purpose, different high-temperature foils, such as (colorless) polyimide, are being investigated for a-Si TFTs [2], [54], [55] and for LTPS TFTs by optimizing process conditions [56]. As a final note, low-temperature foils are also being investigated for a-Si TFTs [57].

1.2 Large Area Sensors and Circuits (On Foil)

Besides displays, there are a variety of application domains that also benefit from the fast progress in TFT research driven by display applications. X-ray imagers are an example that requires a TFT backplane [1] and where the research field currently explores the option of flexible X-ray detector arrays [58]. Moreover, TFT technologies developed for flexible substrates may provide options for flexible smart systems and lower-end digital electronics.

Conventional monocrystalline silicon complementary metal-oxide-semiconductor (CMOS) technologies would easily meet the technical specifications for the applications named, such as power consumption, operational frequency, and low supply voltages. However, specifications such as low cost, large area, or flexible substrates will be difficult to obtain for monocrystalline silicon CMOS. TFT technologies, on the other hand, enter the picture when a low-cost technology per unit area is required, possibly fabricated on flexible substrates. Monocrystalline silicon CMOS technologies are currently being manufactured on 300 mm substrates targeting 450 mm as a next baseline. Thin-film transistor backplanes in contrast are fabricated on large glass plates. The size of such plates has been increased in different generations, leading to the possibility to produce larger displays. This trend is beneficial from a cost perspective, since more displays of the same size can fit on a larger substrate. A generation 8 glass substrate measures 2160 × 2460 mm^2, which may already suit a variety of large area applications. Monocrystalline silicon CMOS technologies are certainly in the lead in terms of cost per transistor, since downscaling of each technology node results in ever more transistors per unit area. TFT technologies cannot compete in achieving this extreme low cost per transistor; on the other hand, the cost per unit area to manufacture a TFT backplane is substantially lower. Moreover, solution-processing of organic and eventually metal-oxide TFTs offers a perspective to evolve toward printed low-cost electronics [1], [19].

Also in the world of ambient intelligence and the Internet of things, flexible smart systems have their place. Sensors, actuators, and cryptographic and other electronic functions can all be integrated on foil, illustrated in Figure 1.1. The integration of an AMOLED display on passports is one example of such a flexible smart system [59]. As another example, Someya et al. have demonstrated a flexible pressure sensor matrix on a large area driven by organic TFTs for artificial skin applications [60].

Integration of electronics with sensors on foil requires an efficient *analog* sensor interface. In recent years, the first analog-to-digital converters based on organic TFTs have been demonstrated [61], [62]. The digital signals from the analog-to-digital converter could be analyzed by lower-end digital electronics before storage or transmission via RF interface. A first 8-bit, flexible microprocessor realized with organic transistors that can execute basic signal analysis has been demonstrated [63]. This microprocessor is described in detail in Chapter 6.

A big driver in the field of organic and printed electronics is the application domain of radio-frequency identification (RFID) tags. When the price of such

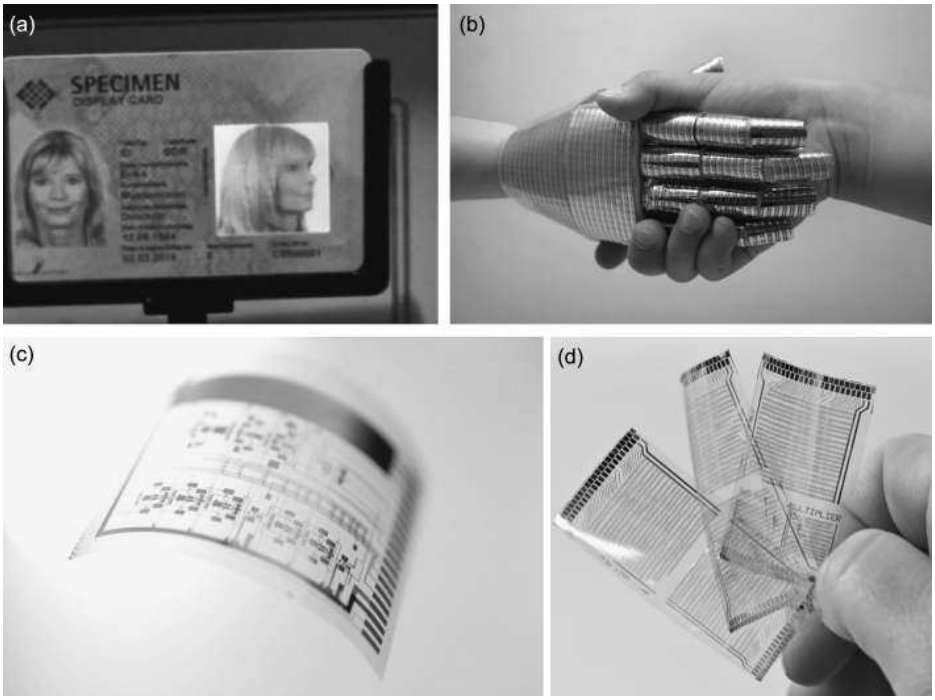

Figure 1.1 (a) Integration of an AMOLED display on passports [59]; (b) example of an artificial skin application [60]; (c) flexible, organic analog-to-digital converter [64]; and (d) 8-bit organic microprocessors on foil [63].

RFID tags can be reduced below $0.01, the targeted application can be item-level tagging. In that case RFID on foil can eventually replace barcodes cost effectively. Organic or metal-oxide RFID tags can be used as anti-counterfeit protection, in ski passes, and in many other applications. Organic and metal-oxide thin-film transistors exhibit much less intrinsic performance compared to monocrystalline silicon CMOS circuits, for which current RFID standards are designed. A main focus in research toward low-cost, thin-film RFID tags is thus to investigate whether these silicon inspired CMOS standards can be reached with circuits in TFT technologies. Chapter 5 will discuss the design of organic and metal-oxide RFID tags.

The fact that an 8-bit microprocessor and complex analog circuits based on organic electronics have been realized implies that these technologies have reached a certain maturity. The 8-bit microprocessor contains more than 3,000 unipolar p-type, organic thin-film transistors. This level of integration thus allows the integration of basic signal processing functions. Robust logic gates are needed for such realizations. How these can be realized will be discussed in the subsequent chapters of this book.

2 Organic and Metal-Oxide Thin-Film Transistors

Organic and especially metal-oxide thin-film transistors have great potential to be introduced as a backplane technology for next generation displays or imagers, or to be used as a thin-film transistor technology on a large area for circuit and sensor integration. The discussion in this chapter focuses therefore on both technologies that have been used in this book. Primarily, four main device architectures are described. Subsequently, the operational principle of thin-film transistors is briefly explained with and without a back gate. Some typical layout rules and important parasitic capacitors in these technologies are suggested. Next, all six technologies used for the circuit realizations in the following chapters are described. Prior to the Summary, trends in circuit integration for three different circuit topics are discussed. Those three topics are display periphery, digital circuits, and analog circuits.

2.1 Device Configurations

Figure 2.1 provides a brief overview of four main transistor architectures for single-gate thin-film transistors. These architectures can be split into several categories: top-gate versus bottom-gate devices and staggered versus coplanar structures. The main difference between staggered and coplanar architectures is the location of the source-drain electrodes with respect to the transistor's channel. In a coplanar device, the source-drain electrodes are both located at the channel interface of the semiconductor. In the staggered structure, source-drain contacts are made on the opposite semiconductor interface, with the result that injected carriers at the source need to travel through the semiconductor to reach the channel. A staggered structure has a strong vertical field enhancing charge injection from the contacts. This field is shielded by the contacts in a coplanar device, which increases the injection barrier. All devices, except for the bottom-gate coplanar device, require processing on top of the semiconductor. Therefore, the semiconductor needs to be resistant to the next processing steps, when the device architecture differs from bottom-gate coplanar. Many advantages and disadvantages for these transistor architectures are extensively reviewed by Klauk for organic TFTs [19].

Park et al. elaborated on the device structures regarding metal-oxide TFTs [38]. Commonly used is the bottom-gate staggered structure, including a protective layer

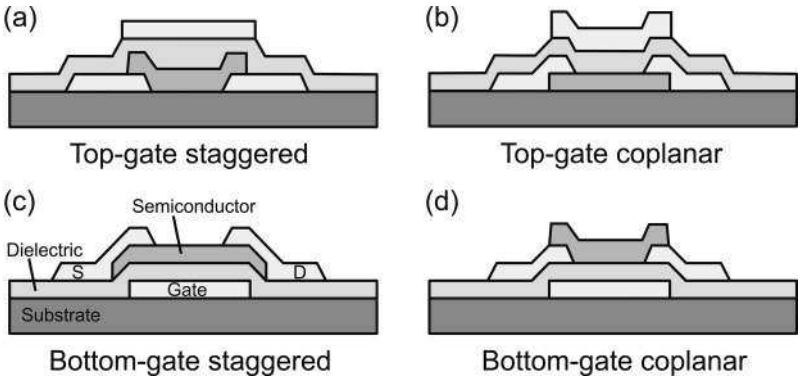

Figure 2.1 (a) Top-gate staggered, (b) top-gate coplanar, (c) bottom-gate staggered, (d) bottom-gate coplanar TFT configurations.

to isolate the back channel surface [38]. This protective layer can be added after formation of the source-drain contacts, which serve as an encapsulation layer, resulting in back channel etch (BCE) devices. Another option is to fabricate this protective layer prior to the definition of the source-drain electrodes in order to protect the back channel from further processing, resulting in etch stopper (ES) devices. ES device architectures are widely used for the fabrication of a-Si backplanes [37], [38]. As an alternative solution, Sony demonstrated in 2012 an AMOLED display based on a self-aligned, metal-oxide transistor backplane with a top-gate coplanar-like TFT [65]. The key advantage of the latter process flow is the reduction of the overlap capacitance between source-drain and gate electrodes resulting in a faster RC time to store data on each pixel.

The devices in this book have been fabricated using the bottom-gate coplanar TFT architecture, for both organic and metal-oxide semiconductors. This device structure requires for organic TFTs proper surface conditioning, both for dielectric and for source-drain contacts, in order to enhance the electrical properties of the transistor [19]. In many cases, the semiconductor has been protected for moisture by an additional encapsulation layer.

2.2 Operation Principle

2.2.1 Operation Principle of a Single-Gate Transistor

A transistor acts as an electrical switch of which the resistance depends on the voltage applied to the gate electrode. Transistors made in a classical bulk semiconductor (e.g., silicon) usually operate in inversion: source and drain diodes are in this case formed by implantation in the semiconductor of the dopant, which provides the opposite charge carrier compared to the dopant of the bulk of the semiconductor. The gate electrode is subsequently biased such that similar opposite charges are