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Part VIII Appendix: VHDL coding style and syntax guide

**Appendix A: VHDL coding style**

A.1  Basic principles  
A.2  All state should be in explicitly declared registers  
A.3  Define combinational design entities so that they are easy to read  
A.4  Assign all signals under all conditions  
A.5  Keep design entities small  
A.6  Large design entities should be structural  
A.7  Use descriptive signal names  
A.8  Use symbolic names for subfields of signals  
A.9  Define constants
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