1 Introduction to electronic package engineering

Over the last few decades, major advancements in the semiconductor supply chain have occurred. These advancements have provided standard foundry processes, physical theories that explain device models, accurate and efficient software, and test equipment. Today, front-end components up to 95 GHz (E-band) and beyond are either commercially available or can be specifically commissioned. In all these advancements, packaging has been the one area where investments and technology have lagged.

In many cases, packaging presents the major bottleneck to overall performance. As trivial as the connection of components may sound, the unfortunate reality is that the signal integrity of interconnects quickly limits performance at high frequencies. Engineers in the digital world are now coming up against some of these limitations, and only recently has the field made the investments necessary for these signal integrity issues to be overcome. Even microwave engineers, whose whole world is high frequency, struggle to find acceptable packaging solutions. Many will be faced with designs riddled with crippling mismatch loss, coupling loss, and unacceptable resonances.

For many engineering projects, cost is also an important design criterion and differentiating feature. Without careful, directed analysis, engineers may find their projects behind schedule and over budget. Further, lower operating costs can be achieved with package designs that encourage simple fabrication, assembly, handling, and test. Packaging research helps to advance new design techniques and package processes. For these reasons, packaging is rapidly gaining attention as a necessary growth field.

Liquid crystal polymer (LCP) is a new material that has emerged as a "holy grail" which could hold the key to a packaging revolution. It is a plastic with barrier properties similar to ceramic crystal. Since LCP is a plastic, multilayer structures using it are easy to process at low cost. Because it has crystal properties, this material exhibits low electrical losses, is near-hermetic, and has low moisture absorption and mechanical flexibility properties. This chapter is intended to provide a basic overview of high-frequency packaging. In section 1.1 we briefly discuss various packages that were previously popular but may not be suitable for high-frequency operation. Section 1.2 lists common packaging requirements. Then, in section 1.3 we describe the general process flow for package design.

1.1 A brief discussion of standard packages

Countless package types exist, but most fall into a few different standardized package styles. At low frequencies, i.e. < 1 GHz, plastic packages such as a single/dual in-line package (SIP/DIP) or a small-outline integrated circuit (SOIC) are used. A DIP is mounted by inserting its two parallel pin rows through contact vias on a mother board. An SOIC package is similarly mounted, by soldering its leads to motherboard pads. As the application frequency increases, these packages become unsuitable. In a DIP a number of features, including the bond wire connections, package lead legs, and solder joints, present features that are detrimental to electromagnetic power transmission at high frequencies. Further, DIP and SOIC package leads have lengths on the order of several millimeters. At microwave frequencies these features are electrically large (i.e. greater than one-twentieth of a wavelength) and cause significant mismatch. Further, the above-mentioned packages are not precisely defined in regard to their dimensions on the motherboard when mounted. These large tolerances make high-frequency use impossible. To get an idea of the scale, one-twentieth of a wavelength at 6 GHz corresponds to 2.5 mm. At 60 GHz, one-twentieth of a wavelength corresponds to 250 μm, which is shorter than most advanced wire bonds. Hence, it is apparent that RF packaging requires greater consideration as operating frequencies increase.

Efficient signal power transfer requires an equivalent matched (typically 50 Ω) transmission line between source and destination. As operating frequencies increase, this becomes difficult owing to proportionally challenging distributed transmission line effects. Compensating these parasitic effects becomes very difficult with the limited space inside a package and/or on a motherboard. Other metal-can-type packages, such as TO-8, suffer similar frequency limitations. Quad flat packages (QFPs) and pin grid arrays (PGAs) are generally formed with shorter leads (or pins) to minimize parasitics and increase input/output density. These types of package may offer reasonable performance. It is possible to use such leaded packages at high frequencies in non-hermetic applications.

To remove lead parasitic effects completely, leadless packages have been developed that are attractive for higher-frequency work. Leadless packages in rough chronological order of their appearance include ball grid array (BGA), quad flat no-lead (QFN), land grid array (LGA), flip-chip, and wafer-scale packages. These packages have recently been adopted as a JEDEC standard, and they are at the forefront of advanced packaging research. A BGA package contains a rectangular surface on which the leads have been replaced with solder balls. This package is surface mounted (SMT). Lead elimination greatly reduces inductance from bumps and package pad connections as compared with that found with in-line and small-outline integrated circuit (SOIC) packages. Similarly, QFN and LGA technologies are packages with metal surfaces exposed for contact in SMT application. The QFN and LGA technologies differ, as one has contact pads along the periphery while the other has pads arrayed across the entire surface. The QFN package may be formed with an over-mold lead frame or printed as an organic substrate, while

LGAs are only available in the latter style. Flip-chip packaging involves attaching a die with bumps that directly attach the die pads to the board. Bumps are formed of either solder with a controlled collapse chip connection (C4) process or gold bumps formed using ball bonders. Additional mechanical support is optionally provided with under-fill material. When diced, the individual packaged chip is the same size as the die. Lastly, wafer-scale packaging consists of laminate film placed on a wafer to form interconnects and may be mounted by means of either the SMT or the flip-chip method. Today, a number of chips are packaged in these technologies because they offer lower costs, smaller form factors, and higher-frequency performance over their leaded predecessors; LCP can and will be shown to have unique advantages when one is building these types of package.

1.2 Package design requirements

One goal for package engineers is to make a package transition look like a 50 Ω through line. Electrical interconnects need a 50 Ω matched package transition to reduce power reflections. In this book, an electrical interconnect from chip to PCB will be referred to sometimes as a package *feed-through*. In any feed-through design, there are conductor and dielectric losses that contribute to the total loss. These losses are due in large part to the material used; LCP is one material that provides low-loss performance. In order to discuss losses for high frequencies, one needs to use S-parameters, the most common electrical measure of package performance. They will be reviewed insofar as they relate to electrical packaging in section 1.2.1, in an intuitive manner. Other common requirements in package design besides electrical performance and material involve weight (section 1.2.2), size (section 1.2.3), thermal effects (section 1.2.4), and reliability (section 1.2.5).

1.2.1 Electrical requirements

To characterize power transfer characteristics, S-parameters are used in lieu of *Z*-parameters since *scattering* becomes a more practical metric to characterize in a consistent 50 ohm termination system. The *insertion loss* (IL) is the decibel form of the ratio S21 of the output at port 2 and the input at port 1. Thus we have

$$\mathrm{S21} = \frac{\text{power out of port 2}}{\text{power into port 1}}, \tag{1.1}$$

$$\mathrm{IL} = -10 \log \mathrm{S21} = -10 \log\left\{\frac{\text{power out of port 2}}{\text{power into port 1}}\right\} \ \text{(dB)}, \tag{1.2}$$

where the powers are in absolute values, i.e. watts (W). Insertion losses are often tracked to within 0.1 dB accuracy. At any juncture, power entering port 1 either can be (1) transmitted through to port 2, (2) reflected back to port 1, or (3) dissipated

in between port 1 and port 2. Note that in a microwave package there is no strict convention for port designation, but typically port 1 is used to indicate the input. The S-parameters should be accompanied with port-definition information when three or more port networks are characterized. Transmission lines have losses that are largely dominated by conduction loss and dielectric loss. Conduction loss generally dominates at low frequency and is proportional to the square root of the frequency. Dielectric loss is proportional to frequency and hence may become the dominant loss mechanism at sufficiently high frequencies. Other, usually negligible, loss effects include radiation and dielectric conduction loss. For packaging, one goal is to minimize insertion loss at desired frequencies.

Another important parameter to consider is the *return loss* (RL), which is represented by S11 where

$$\mathrm{S11} = \frac{\text{power out of port 1}}{\text{power into port 1}}; \tag{1.3}$$

the return loss is then given by

$$\mathrm{RL} = -10 \log \mathrm{S21} = -10 \log\left\{\frac{\text{power out of port 1}}{\text{power into port 1}}\right\} \ (\mathrm{dB}). \tag{1.4}$$

The return loss thus measures the amount of power reflected from a port. Backward power reflections are unacceptable, and can cause component damage, in many systems. Generally, however, for packaging the goal is to maximize the return loss or, in other words, to have a large negative S11 value. Many commercial components specify a 10 dB return loss. However, junction mismatches can add up in a phenomenon known as voltage standing wave ratio (VSWR) stacking. For junctions with a reasonable return loss, VSWR stacking may cause a worst-case return-loss degradation of 6 dB. For instance, back-to-back junctions, each with a 20 dB individual return loss, may give only a 14 dB combined return loss at some frequencies. For this reason, one often needs to design packaging with a much higher return loss than that required by the total system specification.

In package interconnects, a significant portion of the insertion loss can be attributed to the mismatch loss (ML), given as

$$\mathrm{ML} = -10 \log[1 - (10^{-\mathrm{RL}/20})^2] \ (\mathrm{dB}) \tag{1.5}$$

where RL is in dB units. For example, a 10 dB return loss has a 0.46 dB associated mismatch loss.

One way to improve the return loss is to add attenuating elements. This improves return loss at the expense of insertion loss. For example, consider the case of adding a 3 dB attenuator in front of a 10 dB return loss reference plane. The return loss will improve by 6 dB to 16 dB. The reason is that the power is reduced by 3 dB in both the forward and return directions. In this case, the insertion loss is only degraded by

3 dB as a result of forward power attenuation. However, to lower costs and increase performance, more careful package design is required, as we shall discuss.

Cross-talk, also referred to as *isolation*, may be yet another package requirement. Cross-talk generally is given as a large negative decibel value, e.g. –40 dB, while the isolation is reported as the absolute value, here, +40 dB. Cross-talk may be considered a special case of insertion loss where now an undesired signal appears. In this case, the aggressor signal may leak into another part of the package and add unwanted noise.

Other parameters that are relevant to microwave operation are the ABCD-parameters and the T-parameters (which determine the transmission). A number of well-known relations between the S-, ABCD-, T-, and Z parameters can be obtained. Lastly, a variation of the normal S-parameters is presented by mixed-mode S-parameters, which apply to differential systems. In a set of mixed-mode S-parameters, differential and common-mode parameters are both present. For differential signaling, differential S-parameters indicate the useful signal being transmitted. Other parameters relating to common-mode performance can be used during the design process. Again, well-known relations enable one to convert between single-ended and mixed-mode S-parameters.

The noise figure (NF) is an electrical parameter critical to low-noise-amplifier (LNA) and receiver design. The noise figure is directly affected by the electrical packaging, where a package insertion loss in front of the LNA degrades the noise figure by the same amount. In other words, 1 dB of package loss before the LNA correspondingly degrades the NF by 1 dB.

The output power is also directly degraded by any back-end packaging losses. For instance, 1 dB of package loss after a power amplifier (PA) means that maximum output power is reduced by 1 dB. This would mean that a 1 W (30 dBm) PA chip would only offer 0.8 W (29 dBm) after packaging. Note that 0.2 W power is 23 dBm. Also, note that the output-side packaging losses similarly directly degrade the third-order intercept (IP3 or TOI) and 1 dB compression point (P_{1dB}), which are measures of linearity. Hence, packaging can significantly affect electrical performance and has become a major interest of electrical engineers.

1.2.2 Weight requirements

It is well known that lightweight packages are desirable to cut down operation cost in mobile systems such as handsets. Less known is the need to reduce weight in airplanes and ground vehicles. A phased-array radar may be constructed using ceramic packages and weighs about 250 kg in a military vehicle application [9]. Packaging materials such as LCP are attractive for weight-sensitive applications since its mass density is only around 1 gram per cubic centimeter. If ceramic is replaced with LCP then the total weight of a vehicle may be reduced by around 160 kg, and this improves the efficiency of the vehicle. For space applications, lightweight gains are even more significant, where the ratio of the rocket fuel weight and the load must be an overwhelming 100 :1 during launch. Hence, weight can be

a significant criterion for performance, and reduction in weight can lead directly to reduced operation costs.

1.2.3 Package physical requirements

High-density packaging capability is highly desirable. Multilayer structures achieve this by allowing the same footprint to have more functionality. Additional adhesive layers are required to achieve multilayer structures using substrates such as FR4, high-frequency laminates [1], or organic films [2]. Adhesive layers are not guaranteed to have low moisture-absorption characteristics, and this may allow moisture to flow freely into the package cavity. Fortunately, LCP allows for multilayer laminated builds, has a low moisture uptake, and so provides an ideal match for high-density requirements. LCP is conveniently available in varying film thicknesses (0.5 mil to > 4 mil) with various Cu cladding thicknesses. A common metal thickness for LCP is 1/2 oz (18 μm). Incidentally, while PCB terminology uses "oz" for thickness, it should more appropriately be given as oz/ft^2, referring to the weight of the metal over one square foot. Lastly, other constraints may occur from the limitation in the X, Y, or Z dimensions dictated by the system requirements.

1.2.4 Package thermal requirements

Packaging high-power active components requires thermal management. Performance and reliability degrade when the recommended junction temperatures are exceeded. Further, packages such LGAs are sensitive to mismatch of the coefficient of thermal expansion (CTE) at the epoxy interface between a package and the semiconductor die, which could be around 6 ppm/°C. These packages are also sensitive to CTE mismatch at solder joints between the package and the motherboard (17 ppm/°C). Given that chips are usually quite small compared to the overall package dimensions, it is usually recommended that package materials have a CTE closer to that of the motherboard PCB than that of the die. Thus LCP is attractive as it has a CTE of 17 ppm/°C, which has been engineered to match Cu and PCBs. Further, LCP is a flexible material, so that it can yield easily and may accommodate CTE mismatches without the material cracking. This allows LCP packages to have low solder-joint stresses.

Depending on the particular chip technology, 135, 150, and 175 °C are commonly specified temperatures at which junctions must be maintained in order to provide 10^6 hours of mean time to failure (MTTF) with 85 °C ambient [10]. Emerging microwave chip technologies involving SiC and GaN may have junction temperatures above 200 °C. In order to remove heat from active components, thermal conduction and convection mechanisms may be explored. To reduce junction temperature, one can utilize a copper die-pad that externally conducts heat away from the package. Examples of multilayer thermal schemes are provided later in this book. In a scheme based on LCP, a cavity is drilled entirely through soft LCP dielectric so that a chip sits directly on a thin copper surface to allow efficient heat

dissipation. Convection can also be used to cool packages with either passive circulation as heat rises, or active forced-air cooling to remove heat. Heat sinks are commonly used to provide a large stable material that can be conveniently temperature regulated and monitored. Heat sinks can also be machined to allow greater surface area for convection cooling and are commonly incorporated outside the package design. Thermoelectric coolers (TECs) based on the Peltier effect may also be used to cool packages. In this method, electric current facilitates the removal of heat through a semiconductor junction. Note that TECs are usually placed externally to RF package modules, for, placed internally, they would add significant cost and power consumption.

The thermal dissipation in a package may be calculated as the DC power plus the input RF power minus the output RF power. Power density is an important aspect to consider, as thermal concerns are too often limited to the output-stage transistor junctions in a power amplifier chip. This means that a significant amount of power is often dissipated in a very small area of a chip. Hence, for thermal considerations, power and area are important parameters to note during the thermal design of packages. Analysis may be performed to calculate the first-order junction temperature from a knowledge of the material's thermal resistance. For instance, with 15 °C/W thermal impedance from junction to case (θ_{JC}) and 2 W power dissipation, one would expect a 30 °C heat rise from case to junction. With an 85 °C case temperature, the junction temperature is expected to be 115 °C. This may be summarized as

$$T_J = T_C + \theta_{JC} P_{DISS} \quad (^\circ\text{C}), \tag{1.6}$$

where T_J is the junction temperature in °C, T_C is the case temperature in °C, θ_{JC} is the package thermal impedance from junction to case in °C/W, and P_{DISS} is the power dissipation in W. The thermal impedance θ_{JC} may be approximated to first order by the equation

$$\theta = \frac{L}{KA} \quad (^\circ\text{C/W}) \tag{1.7}$$

where L is the length (in m), K is the thermal conductivity in W/(m °C) or W/(m K), and A is the cross-sectional area in m^2. Additional first-order approximations for planar multilayer structures may incorporate heat-spread angles to estimate the thermal impedance [11]. For a more accurate analysis, full three-dimensional simulation tools are available. Additional details on these tools are discussed in section 1.3.

1.2.5 Package reliability requirements

An electronic package should provide long-term reliability and sufficient protection from external environment changes, such as temperature, humidity and pressure or force. Moisture is a significant aggravator degrading electrical performance. When moisture enters a package, it can corrode metal pads or traces on MMICs and the constituents of package and chip materials. These may change electrical

properties, and this may in turn lead to system failures. Therefore, a package material should have very low moisture absorption and permeability in order to stop moisture from entering the package cavity. LCP is known especially for having low-moisture-uptake and hermetic properties. A package is considered to be hermetic if its cavity leak rate is less than 5×10^{-8} atm/(cm^3 s). LCP has been demonstrated by several groups to satisfy this low-leak-rate requirement for hermeticity. It has been demonstrated to satisfactorily package MEMS devices, which are one of the most environmentally sensitive technologies in existence.

Commonly used reliability tests have been standardized by various organizations [6–8]. (Interestingly, despite their imposing sound, military standards may not always be the strictest available for a given type of test.) Since it is impractical to perform every possible test, tests are selected on the basis of potential reliability concerns as determined by engineering experience. The tests selected are often based on those that historically have been performed for similar products. Common tests include thermal cycling, life testing, and highly accelerated stress testing (HAST). More specifics on actual tests are provided in Chapter 8.

Reliability testing is often expensive and time-consuming; some tests need to run for several months. A number of vendors offer services to perform these tests and are glad to offer their inputs. Ideally, every manufactured package would be put through the same gauntlet of tests; however, in order to save time, money, and allow faster time to market, a method known as "qualification by similarity" may be performed. This builds on prior successful qualification efforts on like packages. When conducting qualification by similarity it is important to confirm that the package being considered is actually similar in form and manufactured by the same suppliers. Qualification by similarity is only valid for less challenging package designs and is generally possible for packages slightly smaller than prior-qualified parts. This method should be used carefully and sparingly, as any error in method application may call into question packages previously qualified as well as engineering integrity.

1.2.6 Package material requirements

Ceramic, glass, and metal hybrid packages are frequently used to provide low loss and hermeticity at microwave frequencies. Processes such as low-temperature co-fired ceramic (LTCC) have been developed to lower processing temperature and enable multilayer packaging. Even so, LTCC is still processed at 1000 °C, and in a small size, that may not be cost effective. Furthermore, screen-printed conductor on green tape does not have as high a conductivity as copper, and high-frequency performance is limited owing to losses. Poor thermal dissipation is another disadvantage of ceramic packages. Exceptional ceramics known for good thermal dissipation are aluminum nitride (AlN) and beryllium oxide (BeO), but these materials are extremely costly and suffer from poor fabrication. In the case of BeO, the dust generated from processing is known to be poisonous and may require special disposal.

Low-cost lightweight hermetic packages are needed in order to save space, an important aspect of microwave circuits. Organic materials have a low mass density, around ~1.2 g/cm^3, compared with ceramics, which have mass density 4 g/cm^3. Many low-cost packages are constructed using over mold with plastic. However, such over mold causes electrical detuning of the characteristic impedance and phase and increases the chip junction capacitance. To some degree, such a capacitance increase can actually help offset the electrical package's inductance, but generally it complicates the chip design considerably and is only viable when extremely challenging electrical specifications are being met. Further, their high dissipation factors and affinity to moisture make most plastics unattractive for high-frequency packaging. However, LCP is unique as a thermoplastic for building new, sophisticated, high-frequency packages.

1.3 Package design process

In this section we provide a generic set of instructions that should serve the reader undertaking a new package design. It is our hope that the packaging industry can benefit from standardization, which has served to advance the electronics industry as a whole. Package design often begins with technology selection. Then, drawings are created to specify how the package will appear. Electromagnetic and circuit simulations are conducted. Lastly, physical packages are built and tested. Any experienced engineer can attest that it is necessary to iterate within and across the steps outlined above. Also, note that this section focuses on the package or module build. There are additional considerations such as the assembly of electronics into the package, and many vendors are ready to provide guidance.

1.3.1 Technology selection

The process to design a package often begins with technology selection. It is in this first step that the material properties and physical capabilities are clarified. Often a selection is made on the basis of institutional experience combined with ad hoc changes of certain features, depending on what the market offers. Once a process is selected, the engineer must identify package manufacturers and obtain a set of design rules. Non-recurring engineering (NRE), volume unit pricing, and lead times are important, and should be discussed, for any engineering project.

Unlike in the case of semiconductor foundries, package design rules are often not prepackaged for a customer. Often it is up to the engineer to discuss needs and see whether a particular concept is viable. Common parameters and dimensions of interest include the minimum signal width, the gap, the via diameter, pad, anti-pad, pitch, and the material thicknesses.

Ceramic packaging is considered highly reliable in regard to thermal and hermetic requirements. Common ceramic package materials include alumina (Al_2O_x), beryllium oxide (BeO), and aluminum nitride (AlN). The drawbacks of ceramic

packages are that they are generally bulky, expensive, have high dielectric constants, and suffer from shrinkage, which limits the precision of the final package dimensions. The shrinkage can be as much as 20% in length, depending on the specific process conditions. An absorber may also be required to be inserted if package resonances are an issue. Ceramic packages are created as air cavities and may either be dominantly metal or ceramic along the edge surface. Once a package is available, the electronics are assembled and lid sealing is performed. This is often done using seam sealing, which involves rollers that conduct a high electrical current to heat and melt the metal lids along their edges.

Plastic packaging is another technology highly regarded for being low cost and easy to process. Packages may either be air-cavity formed or fully over molded. A large number of plastic varieties are readily available. The metal for signals can be provided through printing or lead frame techniques. The drawbacks of plastic packages include high dielectric loss and non-hermetic characteristics, which can lead to moisture ingress and popcorning. Owing to the process limitations of plastics, it can be difficult to obtain precise physical features down to 100 μm. Further, over-mold parts may be sensitive to wire sweep owing to the possibility of plastic flow.

Direct chip attach (DCA) is yet another package technology that has the benefit that it can be made with low-cost printed circuit board (PCB) [5]. In DCA, electrical chips can be directly mounted onto PCB. Direct chip attach techniques encompass chip-on-board (CoB), chip-on-flex (CoF), chip-on-glass (CoG), and flip-chip and have been used to realize a number of package form factors including land grid array (LGA) and QFN. Depending on the application, DCA can present assembly challenges and can give rise to CTE chip-to-substrate or substrate-to-motherboard mismatches.

For ceramic, plastic, and DCA packages we would invite the reader to consider LCP as a viable alternative to any of the processes considered in this subsection; the quest for hermetic organic surface mount packages has led to the investigation of LCP for packaging. It has a permeability close to that of glass and can be used to construct hermetic cavities. Further, it retains most of plastic's benefits as a low-cost packaging solution. One concept using LCP for a highly functional system-in-package (SiP) is illustrated in Fig. 1.1. This book will go into the details of why LCP is an appropriate choice that offers most of the benefits presented by ceramic and plastic technologies.

1.3.2 Computer-aided design (CAD)

Once the general package concept and associated design rules have been determined, a model package must be drawn and analyzed. Manufacturers should specify the electronic formats that they can accept. Common formats include AutoCAD(.dxf) and Gerber. In these cases it may be necessary to do somewhat redundant work, namely to draw package models for both manufacturing and electromagnetic design purposes. Standardization and sophistication are increasing, and there is now a push to align these tasks better. As package houses become more sophisticated,