Digital Front-End in Wireless Communications and Broadcasting

Circuits and Signal Processing

Covering everything from signal processing algorithms to integrated circuit design, this complete guide to digital front-end is invaluable for professional engineers and researchers in the fields of signal processing, wireless communication, and circuit design. Showing how theory is translated into practical technology, it covers all the relevant standards and gives readers the ideal design methodology to manage a rapidly increasing range of applications. Step-by-step information for designing practical systems is provided, with a systematic presentation of theory, principles, algorithms, standards, and implementation. Design trade-offs are also included, as are practical implementation examples from real-world systems. A broad range of topics is covered, including digital pre-distortion (DPD), digital up-conversion (DUC), digital down-conversion (DDC), and DC-offset calibration. Other important areas discussed are peak-to-average power ratio (PAPR) reduction, crest factor reduction (CFR), pulse-shaping, image rejection, digital mixing, delay/gain/imbalance compensation, error correction, noise-shaping, numerically controlled oscillator (NCO), and various diversity methods.

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Contents

List of contributors *page* xii
Preface xvii

Part I Introduction to digital front-end 1

1 Introduction to wireless communications and digital broadcasting
Hongxiang Li, Guanying Ru, Siqian Liu, Hui Liu, and Jenq-Neng Hwang 3

1.1 Evolution of mobile cellular networks 4
1.2 Evolution of broadcast network 9
1.3 Key technologies 15
1.4 Conclusions 23
References 24

2 Basic principles and protocols of digital wireless communications
Dimitra I. Kaklamani and Panagiotis K. Gkonis 28

2.1 Introduction 28
2.2 Digital processing, transmission, and reception 29
2.3 The WCDMA/OFDMA physical layer protocols 32
2.4 General principles of MIMO systems 39
2.5 Space-time and space-frequency transmission over MIMO networks 44
2.6 Summary 48
References 48

3 Digital front-end and system overview in wireless communication
Eduard Bertran and Maurizio Pagani 50

3.1 Introduction 50
3.2 New objectives and technologies in modern wireless communication systems 56
3.3 Other emerging standards beyond 3G 76
3.4 DFE introductory design considerations 79
3.5 Conclusions 91

List of abbreviations (Chapter 3) 91
References 95

4 System overview and front-end technologies in digital broadcasting
Francesc Tarres and Eduard Bertran 98

4.1 Introduction 98
4.2 Broadcast mobile multimedia services 102
4.3 Common technologies for digital mobile broadcast services 103
4.4 Most relevant standards for digital broadcasting to mobile devices 105
4.5 Technology aspects of DFE in transmitters 111
4.6 Conclusions 116
List of abbreviations (Chapter 4) 116
References 118

5 Digital front-end for multiple standards and multimode compatibility
Eduard Bertran 120

5.1 Introduction 120
5.2 Receiver architectures 122
5.3 Analog-to-digital converters 126
5.4 Preselect filters and LNA interface for multiband receivers 128
5.5 Power amplifier architectures in multimode-multiband transmitters 130
5.6 Conclusions 135
List of abbreviations (Chapter 5) 136
References 137

Part II DPD and CFR 141

6 General principles and design overview of digital predistortion
R. Neil Braithwaite 143

6.1 Introduction 143
6.2 Power amplifier nonlinearity 143
6.3 Digital predistortion overview 150
6.4 Digital predistortion basics 160
6.5 Advanced topics in DPD 177
6.6 Concluding comments 187
References 189

7 Power amplifier nonlinear modeling for digital predistortion
Gabriel Montoro and Pere L. Gilabert 192

7.1 Introduction 192
7.2 Principles of predistortion linearization 193

7.3 Power amplifier behavioral models for digital predistortion 196
7.4 Discussion 210
References 211

8 Look-up table based digital predistortion schemes and implementation
Pere L. Gilabert and Gabriel Montoro 214

8.1 Introduction 214
8.2 Look-up table based schemes 215
8.3 FPGA implementation of an LUT-based DPD 219
8.4 Discussion 240
References 241

9 Digital predistortion and its combination with crest factor reduction
Anding Zhu 244

9.1 Principles of operation 245
9.2 DPD models 246
9.3 Model extraction structures 255
9.4 Bandwidth and sampling rate requirements 257
9.5 System characterization procedures 259
9.6 Implementation considerations 264
9.7 Combination with crest factor reduction 270
9.8 Conclusions and future outlook 276
References 277

10 Adaptive digital baseband predistortion: design and implementation
Hua Qian and G. Tong Zhou 280

10.1 Introduction 280
10.2 Power amplifier nonlinearity behavior and modeling 281
10.3 Digital predistortion modeling 286
10.4 Predistortion implementation challenges 298
10.5 Conclusions 305
References 305

11 Crest factor reduction techniques
Nuno Borges Carvalho and Wohoon Jang 309

11.1 Introduction 309
11.2 Multi-carrier communication systems 311
11.3 CF reduction using clipping plus filtering 319
11.4 Conclusion 326
References 326

Part III DUC, DDC, ADC, DAC, and NCO 331

12 Digital down-conversion and up-conversion: theory and implementation
Yue Zhang, Taiwen Tang, Kok-Keong Loo, Ben Allen, and Dayou Li 333

12.1 Introduction 334
12.2 Multi-rate, multi-stage, and filter-banks in DDC and DUC 339
12.3 Mixing and combining for multi-channels and multi-carriers 348
12.4 Hardware implementation for digital down-conversion 352
12.5 Hardware implementation for digital up-conversion 370
12.6 Summary 377
References 378

13 A/D and D/A data conversion for wireless communications transceivers
Jerzy Dąbrowski 380

13.1 A/D conversion in RF receiver 381
13.2 ADC for heterodyne and low-IF receiver 386
13.3 Digital down-conversion 389
13.4 Implementation of ADCs in communications receivers 392
13.5 D/A conversion in RF transmitter 397
13.6 Digital up-conversion 402
13.7 Implementation of DACs in communications transmitters 402
13.8 Summary 409
References 410

14 Advanced quadrature sigma-delta modulator designs for A/D interface
Mikko Valkama, Jaakko Marttila, and Markus Allén 413

14.1 Sigma-delta basics 413
14.2 Considerations on further modulator concepts 427
14.3 Advanced modulators 431
14.4 Nonidealities in quadrature sigma-delta modulators 434
14.5 Examples on complex multiband transfer function design 439
14.6 Conclusion 445
References 446

15 Digital suppression of A/D interface nonlinearities
Mikko Valkama, Markus Allén, and Jaakko Marttila 450

15.1 Introduction to ADC nonlinearities 452
15.2 Look-up table 456
15.3 Dithering 458
15.4 Model inversion 459
15.5 Adaptive interference cancellation 460

15.6 Clipping compensation using interpolation 465
15.7 Performance examples of online post-processing methods 467
15.8 Conclusions 470
References 471

Part IV Digital calibration, imbalance compensation, and error corrections 473

16 Digital compensation and calibration of I/Q gain and phase imbalances
Lauri Anttila, Yaning Zou, and Mikko Valkama 475

16.1 Introduction 475
16.2 I/Q modulation and direct-conversion radio architecture 476
16.3 I/Q imbalance signal modeling 477
16.4 Compensation and calibration methods 482
16.5 Design and testing examples 494
16.6 Conclusions 497
References 498

17 Joint digital predistortion of I/Q modulator and power amplifier impairments
Mikko Valkama and Lauri Anttila 502

17.1 Introduction 502
17.2 Effects of IQM impairments on PA intermodulation products and predistorter estimation 504
17.3 Joint PA and IQM predistortion 510
17.4 Predistorter parameter estimation 514
17.5 Simulation and measurement examples 519
17.6 Conclusions 527
References 528

18 Diversity and error compensation in OFDM transceivers: principles and implementation
Tomohisa Wada 531

18.1 Introduction 531
18.2 OFDM transceivers: principles and design 532
18.3 Adaptive antenna array and diversity 547
18.4 Error detection and compensation 556
18.5 Hardware implementation and system integration 563
18.6 Conclusions 571
References 571

19 Front-end architectures and impairment corrections in multimode and multi-antenna systems 573
Guillaume Villemaud, Jacques Verdier, Matthieu Gautier, Ioan Burciu, and Pierre-François Morlat

19.1 Introduction 573
19.2 State of the art of multi-* receivers 574
19.3 Mixed analog–digital front-end architecture for multiband simultaneous reception 580
19.4 Some methods for simplifying analog parts of multi-antenna front-ends 585
19.5 Front-ends combining multiband and multi-antenna capabilities 591
19.6 Conclusions 598
References 599

Part V Circuits and system integration in digital front-end 601

20 Integration and interface of digital front-end with analog front-end 603
Steven Loh

20.1 Introduction 603
20.2 Mixed signal transceiver architectures 604
20.3 Digital–analog system integration and interfaces 610
20.4 Conclusions and discussions 618
References 619

21 Circuits and systems for digital front-ends to support multiple wireless standards 620
Imtinan Elahi and Khurram Muhammad

21.1 Introduction 620
21.2 Major Functions of the DFE 621
21.3 Determination of DFE specifications 622
21.4 Design of DFE to support WCDMA and GGE 626
21.5 Considerations to support LTE 646
21.6 Conclusions 648
References 648

22 Programming models and implementation platforms for software defined radio configuration 650
Tanguy Risset, Riadh Ben Abdallah, Antoine Fraboulet, and Jérôme Martin

22.1 Introduction 650
22.2 Programming environment and tools for SDR 650
22.3 An existing radio virtual machine implementation 658
22.4 Conclusion 668
References 668

23 Programmable discrete-time integrated receiver front-ends
Norm Filiol, Robert Klett, and Thomas Riley 671

23.1 Background 671
23.2 Theory 675
23.3 Zero intermediate frequency receivers 684
23.4 Low intermediate frequency receivers 688
23.5 Case study of a super-heterodyne AM/FM radio receiver 692
23.6 Summary and conclusions 703
23.7 Acknowledgements 704
References 704

24 Multi-port front-end and transceivers for V-band multi-gigabit/s communication systems
Serioja Ovidiu Tatu, Emilia Moldovan, and Sofiene Affes 707

24.1 Introduction 707
24.2 Multi-port interferometer theory 709
24.3 Multi-port V-band practical implementation, modeling, and analysis 718
24.4 Proposed transceiver architectures 722
24.5 Advanced system simulations 727
24.6 Conclusion 731
References 731

25 Cross-layer design and digital front-end for cognitive wireless link
Matthieu Gautier, Guillaume Villemaud, Cedric Lévy-Bencheton, Dominique Noguet, and Tanguy Risset 733

25.1 Introduction to flexible cognitive wireless link 733
25.2 A high-level optimization for SDR: multimode relaying 736
25.3 Implementation of the PHY sensing block: example of TV white space sensing 747
25.4 Conclusion 755
References 756

Index 758

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Preface

With the rapid development and worldwide deployment of broadband wireless communication and digital broadcasting infrastructures, the use of digital processing technology in the front-end and radio frequency unit is growing explosively. Digital processing technology for front-end in transmitters and receivers of wireless communication and digital broadcasting covers a broad range of topics including digital predistortion (DPD), digital up-conversion (DUC), digital down-conversion (DDC), DC-offset calibration, peak-to-average power ratio (PAPR) or crest factor reduction (CFR), pulse-shaping, delay/gain/imbalance compensation, noise-shaping, numerically controlled oscillator (NCO), and conversion between the analog and digital domains. These digital processing technologies offer a number of advantages in power efficiency, cost reduction, time-to-market, and flexibility for software defined radio (SDR) so as to support multiple standards and multimode applications. Unlike baseband processing, front-end is tightly connected to the radio frequency layer, therefore it imposes great limitations and difficulties on digital processing speed, memory, computational capability, power, size, data interfaces, and bandwidths. This suggests that digital processing and circuit implementation of front-end are very challenging tasks and require the huge efforts of the related industry, research, and regulatory authorities.

From an application and implementation design point of view, this book aims to be the first single volume to provide a comprehensive and highly coherent treatment on digital front-end and its system integration for multiple standards, multi-carrier and multimode in both broadband communications and digital broadcasting by covering basic principles, signal processing algorithms, silicon-convergence, design trade-off, and well-considered implementation examples.

This book is organized into twenty-five chapters in five parts.

Part I Introduction to digital front-end

The first part consists of five chapters aiming to present overviews of all the processing components of the digital front-end in both transmitters and receivers of broadband wireless communications and digital broadcasting with emphasis on orthogonal frequency-division multiplexing (OFDM) based systems. General principles and basics of digital wireless communications and digital broadcasting are also provided in the

first two chapters. Chapter 1 first reviews the wireless evolution by looking at two major applications: cellular networks and TV broadcast networks. Then the discussion of Chapter 1 focuses on some key techniques including multiple-input multiple-output (MIMO) technique, OFDM, and cognitive radio. The purpose of Chapter 2 is mainly to provide an overview of the basic principles and protocols of digital transmission in wireless networks. The emphasis of this chapter is on transmission over MIMO networks with space-time and space-frequency transmission techniques being presented in alignment with the WCDMA/OFDMA physical layer protocols.

Chapter 3 is devoted to the front-end and system overview of broadband wireless communications. Firstly digital front-end and its key processing units are reviewed. Then this chapter presents new objectives and technologies for transmission and reception of modern wireless communication systems with emphasis on the front-end part. In particular, this chapter introduces some recent mobile communications standards, suitable for SDR developments because of their novelty and capability of reconfiguration including the standards in development under the umbrella of the IMT-Advanced Program. Also, this chapter addresses some new standards on the basis of cognitive radio strategies. More importantly, this chapter focuses on various aspects of how to design and implement digital front-end, covering transceivers and related power amplifiers, chip circuits, and their hardware processing platforms.

Chapter 4 presents a system overview and front-end technologies in digital broadcasting. Concepts such as multicast, return channel, video quality, and transcoding are presented in the context of broadcast mobile multimedia services, covering common modulation technologies, different alternatives for audio and video coding, most relevant standards, and proprietary systems for digital multimedia broadcasting. However, the emphasis of this chapter is on key technologies such as analog-to-digital conversion (ADC), digital-to-analog conversion (DAC), DDC, DUC, and power amplifier linearization for digital front-end processing in broadcast transmission and reception.

Digital front-end processing has begun to play an increasingly important role in wireless communication and broadcasting systems to support multiple standards and multimode compatibility, which is the focus of Chapter 5. In this chapter, an overview of the key structures of digital front-end for multiple bands and multiple modes is first presented. Then, this chapter outlines some important aspects regarding the analog-to-digital conversion for multimode and multiband applications as well as the preselect filters and low-noise amplifier (LNA) interface in multimode-multiband transmitters. Power amplifier architectures in multiple standards are also addressed at the end of this chapter.

Part II DPD and CFR

Six chapters in Part II mainly deal with principles, theory, algorithms, circuit designs, and hardware implementations on various computing platforms for digital predistortion and crest factor reduction so as to compensate for power amplifier nonlinearities and to reduce peak-to-average power ratio. With a tutorial style, Chapter 6 presents general principles and design overview of digital predistortion techniques. Chapter 6 first reviews

various nonlinear behaviors and their modeling of a power amplifier (PA) as well as the impact of the nonlinearity on the output spectrum and entire performance of a PA taking memory effects into account. Moreover, this chapter is devoted to providing the details of the basic algorithms, learning-rules, and model selections in designing and implementing a DPD scheme, and also provides comprehensive discussions on some advanced topics in digital predistortion technology.

Modeling of power amplifiers with nonlinearity and/or memory effects is the starting point to develop effective and practical digital predistortion algorithms and hardware implementations, which is the focus of Chapter 7. In this chapter, a comprehensive overview of the most widely used PA behavioral models is first presented on the basis of neural network modeling and Volterra series based modeling methods also taking dynamics of PA into account. Chapter 7 then provides various adaptive algorithms to estimate the parameters (coefficients) of these models so as to make a better compromise among performance, complexity, and accuracy when using these models to obtain the desired DPD schemes.

Chapter 8 mainly deals with look-up table (LUT) based digital predistortion schemes and implementations. The LUT-based DPD has been considered as the most efficient scheme because of its simplicity in computations and circuit implementations. This chapter covers the principles of LUT-based DPD schemes, the LUT organizations (the 1-D or 2-D table architecture), the optimum size of the LUT (trade-off between the data memory size and accuracy), and the indexing and spacing between entries within the LUT. As design references, some implementation examples using an FPGA platform for the LUT-based DPD schemes are also presented in this chapter.

Digital predistortion and its combination with crest factor reduction are addressed in Chapter 9. This chapter first discusses various issues in designing and implementing a practical DPD scheme including model extraction structures, the bandwidth and sampling rate requirements, and system characterization procedures. Then, the chapter introduces some of the widely used crest factor reduction techniques which are proposed to achieve higher power efficiency by reducing the peaks of the transmit signal to a satisfactory level before digital predistortion and allowing a PA to be operated at higher average power.

Chapter 10 is devoted to one of the most important aspects in compensating for the nonlinearity and memory effect of a PA: that is, design and implementation of adaptive digital baseband predistortion. Through implementation examples and their performance, this chapter covers learning architectures for adaptively modeling nonlinear power amplifiers, adaptive estimation algorithms of DPD coefficients, adaptive DPD architecture designs (filter selection, delay compensation, and signal scaling), and fixed-point implementation issues which take DSP, ASIC, FPGA, or other system-on-chip as computing platforms.

In Chapter 11, crest factor reduction techniques are extensively discussed from design to implementation so as to attack the high PAPR problem encountered in multiband-multicarrier communication and broadcasting systems. This chapter lists various crest factor reduction techniques and makes detailed comparisons in terms of throughput, error vector magnitude (EVM), bit error ratio (BER), and system complexity in order to help readers make the best compromise in designing and implementing a practical CFR scheme.

Part III DUC, DDC, ADC, DAC, and NCO

Organized into four chapters, Part III is devoted to technology and practice of digital up-conversion, digital down-conversion, analog-to-digital conversion, digital-to-analog conversion, and numerically controlled oscillator including re-sampling theory, filtering algorithms, aliasing cancellation, combination, mixing, quantization noise, bit-width effect analyses, circuit designs, and hardware implementations. These are the key processing parts that connect radio frequency signals to baseband signals in all broadband wireless communication and digital broadcasting systems.

Chapter 12 deals with up-conversion of the discrete baseband signal stream into a high-resolution radio signal at the transmitter, and down-conversion of a high-resolution radio signal back into a baseband signal at the receiver by covering the basic principles and functionality of DUC and DDC in relation to conversion between intermediate frequency and baseband with the emphasis on the implementation of the DDC and DUC for standard wireless communication systems. Furthermore, this chapter discusses the multi-rate, multi-stage and filter-banks design, I/Q (In-phase/Quadrature) modulation and demodulation, and NCO design in DDC and DUC.

Chapter 13 discusses A/D and D/A data conversion used in the transceivers of wireless communication systems. For ADC, this chapter covers the fundamental specifications like sensitivity, selectivity, dynamic range (DR), equivalent number of bits (ENOB) and linearity constraints. For DAC, this chapter focuses on the fundamental transmitter specifications which include the EVM and the adjacent-channel-power-rejection (ACPR). To show how to meet the above specifications for practical transceivers in RF application systems, this chapter provides design and implementation examples of the state-of-the-art DAC and ADC using CMOS processes.

Design and implementation of advanced quadrature sigma-delta modulator for A/D interface are addressed in Chapter 14. This chapter first outlines the basics of sigma-delta modulation and then extends the discussions to some further modulator concepts (number of bit, stage and band, and related noise shaping). Next, the selected advanced quadrature structures with multi-stage and multiband are provided. In presenting the illustrating examples and their experimental results, this chapter further deals with implementation and design issues related to nonideal factors such as nonlinearity, jitter, and I/Q imbalance.

Chapter 15 deals with ADC nonlinearities and their digital suppression for radio transceivers. Some significant sources of ADC nonlinearities are first analyzed including gain error, offset error, clipping, differential nonlinearity (DNL), and integral nonlinearity (INL). This chapter then discusses the impact of these nonlinearities on ADC performance and presents several digital processing based methods to suppress them. These digital suppression methods mainly employ look-up table, dithering and model inversion. Moreover, some effective adaptive interference cancellation and interpolation techniques are provided in this chapter giving related performance testing examples.

Part IV Digital calibration, imbalance compensation, and error corrections

In addition to the nonlinearities and nonideal factors discussed in Part II and Part III, a number of other nonideal factors exist in transceivers of wireless communications and digital broadcasting from RF to baseband which include channel imbalance (gain, offset, and delay), I/Q mismatch, and synchronization error (RF, sampling rate, FFT window position, and symbol timing). More importantly, these nonideal factors impact on one another. Hence, more comprehensive digital processing techniques on the basis of joint-level, cross-layer, system-level, diversity (time, array, frequency), and error-tolerance principles are highly desirable in order to simultaneously perform digital calibration, imbalance compensation, and error correction in a practical and efficient way. This is the topic addressed in the four chapters of Part IV.

Chapter 16 is devoted to digital compensation and calibration of the I/Q gain and phase imbalances which are the main resource of the resulting mirror-frequency interference in direct-conversion type radio transmitters and receivers. After reviewing the I/Q modulation and direct-conversion type radio architectures, this chapter discusses behavioral modeling of the I/Q imbalance problem in radio transceivers, covering both frequency-independent and frequency-dependent I/Q imbalance cases. Moreover, various approaches for imbalance estimation and calibration are presented with design and testing examples by covering both digital predistortion type techniques on the transmitter side and digital post-correction methods on the receiver side. Also, complete link models including imbalanced transmitter, multipath radio channel, and imbalanced receiver are given in Chapter 16.

In Chapter 17, joint digital predistortion is presented to compensate for both I/Q modulator (IQM) and power amplifier impairments with covering principles, modeling, algorithms, designs, implementation and testing results. This chapter first illustrates that I/Q mismatch and LO leakage interact with PA nonlinearity such that extra intermodulation distortion products appear at the PA output and affect the estimation and performance of PA predistorters provided by the DPD methods listed in Part II of this book. A new predistorter structure is then presented so as to be able to jointly mitigate both IQM and PA impairments including frequency-dependent behavior (memory) of the impairments.

Chapter 18 presents principles and implementation of diversity techniques and various error compensations in OFDM-based transceivers. From a system-level point of view, this chapter first presents the principles and designs of OFDM transceivers and then focuses on adaptive antenna array and several diversity techniques in time-domain, frequency-domain, spatial-domain, and the cross-layer level. Furthermore, this chapter deals with the detection and compensation of various error sources and practical factors. At the end, this chapter presents the hardware implementation in ASIC, DSP, and FPGA platforms with the related chip performance.

The emphasis of Chapter 19 is on radio front-end architectures and related impairment corrections for multiband, multi-antenna, and multimode receivers so as to better support multiple standards and multimode applications. This chapter presents various mitigation

methods of RF impairments such as the phase noise due to local oscillator errors, frequency offset due to error between receiver's and emitter's local oscillators, and IQ mismatches (gain and phase). Different ways of multiplexing signals and sharing resources (hardware, frequency-spectrum, and structure) in multiple band/channel/modes are also described in this chapter.

Part V Circuits and system integration of digital front-end

The last part of this book deals with the system integration, interface, and convergence-to-silicon of digital front-end with analog front-end, baseband processing, and related cross-layer processing to support multiple standards and multimode applications in broadband wireless communication and digital broadcasting. A number of implemented systems are provided in this part to motivate readers that digital and programmable front-end processing can provide better performance, more flexibility, and less-power consumption than analog-based front-end processing and will replace more and more processing parts required from RF to baseband in advanced systems such as MIMO, ultra wideband (UWB), SDR, and cognitive radio.

Chapter 20 describes the integration and interface between the digital front-end and analog front-end focusing on wireless terminals ASICs applications by showing how to minimize costs and size, and also how to optimize power efficiency in designing new devices. This chapter presents several transceiver mixed signal architectures with various analog-to-digital interfaces that have been popularized in today's wireless terminals' ASICs design. Furthermore, this chapter addresses the system aspects of integration and interfaces between digital front-end and analog front-end in detail and also discusses in detail the future directions of these designs.

In Chapter 21, circuits and systems for digital front-end to support multiple wireless standards are addressed with emphasis on receiver front-end. In this chapter, three major functions of digital front-end are first outlined, namely, the sampling rate conversion, channel selection (or filtering), and compensation of various analog/RF impairments. Then, this chapter presents detailed circuit design considerations and system integration specifications of digital front-end to support three major wireless standards: WCDMA, GGE(GSM/GPRS/EDGE), and LTE.

Implementation (computing) platforms and the corresponding programming models are playing a critical role in both digital front-end processing and baseband processing, which is the focus of Chapter 22. This chapter first reviews various platforms and programming models/languages and then presents an efficient programming machine called the radio virtual machine so as to achieve the following functions for SDR dynamic configurations in both baseband processing and digital front-end processing, namely: a programming language that permits an easy expression of physical layers and can be compiled into an executable form (bytecode), an abstraction based on the component model paradigm, mechanism to handle real-time constraints with easy access to hardware, and an arbitrary bit-width arithmetic.

Chapter 23 presents a programmable discrete-time integrated receiver front-end which can greatly reduce the power and other processing costs that are associated with analog-to-digital conversion used in integrated software defined radio. This chapter first discusses sampling theory and various programmable filtering circuits (filter types and transforms, their design and selection). Furthermore, this chapter reviews the programmable zero intermediate frequency and low intermediate frequency discrete-time receiver front-ends outlining the advantages and disadvantages of these receivers. Illustration implementation examples and testing results are also presented in this chapter.

The emphasis of Chapter 24 is on multi-port front-end and UWB transceivers for V-band multi-Gigabit/s communication systems. This chapter shows that multi-port circuits can successfully be used in quadrature down-converters, antenna arrays, and direct modulation of millimeter-wave signals by presenting that the important advantage in using multi-ports is the reduced LO power requested for down-conversion. This is particularly true in millimeter-wave applications where the received RF signal is considerably low, reducing both the cost of LO and the leakage between LO and the RF input.

Chapter 25 presents some algorithms and techniques in designing a flexible or cognitive radio link considering all cross-layer issues from RF, front-end, baseband, and the media-access-control layer. This chapter first introduces four processing steps needed in an SDR transceiver, namely, sensing, analyse, decision, and act; then it presents various advanced algorithms and related implementation examples in performing these four processing steps. How to better use digital front-end processing remains a hot topic in the emerging cognitive radio systems with large number of degrees of freedom and with multimode capabilities. This chapter serves as a starting point for future research and development in this topic.

For whom is this book written?

It is hoped that this book serves not only as a complete and invaluable reference for professional engineers, researchers, manufacturers, network operators, software developers, content providers, service providers, broadcasters, and regulatory bodies interested in broadband wireless communications and digital broadcasting system developments and applications, but also as a textbook for graduate students in circuits, signal processing, wireless communications, microwave technology, antenna and propagation, and system-on-chip implementation.

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