Semiconductor-on-Insulator and Thin Film Transistor Technology
Semiconductor-on-Insulator and Thin Film Transistor Technology

Symposium held December 3-6, 1985, Boston, Massachusetts, U.S.A.

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MATERIALS RESEARCH SOCIETY SYMPOSIA PROCEEDINGS VOLUME 53

MRS MATERIALS RESEARCH SOCIETY  
Pittsburgh, Pennsylvania
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* Invited papers

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Preface

This volume contains selected papers presented at the symposium on "Semiconductor-on-Insulator (SOI) and Thin Film Transistor (TFT) Technology," held in Boston, Massachusetts, December 3-6, 1985. The symposium was organized to assess the progress in SOI material technologies, as well as their applications to VLSI circuits and thin film transistors. Sixteen distinguished scientists were invited to review research activities in seven topical sessions. Fifty-five contributed papers reported on current efforts and recent discoveries in oral and poster presentations. The conference was attended by an international audience representing the USA, France, England, Japan, and China.

The papers in this book have been arranged into five parts. The first three parts, "Zone Melting and Recrystallization," "Heteroepitaxy and Porous Silicon," and "Buried Oxide and Nitride by Implantation," deal with specific approaches for fabricating SOI material and structures. The last two parts, "Characterization of SOI Thin Films" and "Device and Circuit Applications," are more general in scope.

Reports on the zone melt and recrystallization (ZMR) technique in Part I suggest that the long intractable problem of low angle grain boundary formation is at last showing signs of being understood and controlled. Very large area single crystalline silicon thin films, with very low angle "dotted" subboundaries or arrays of isolated dislocations as the only defects, are described in several papers. The best of this material had total dislocation densities between $10^5$ to $10^6$/cm$^2$. This was achieved by empirically choosing the thermal power, scan rate, or patterning method to generate a suitable thermal gradient across the melt–solid interface. A few papers put forth new models of subboundary formation which promise to stimulate further experimental progress. Simulation of heat flow and modeling of molecular dynamics provide more analytical tools to elucidate the mechanism of ZMR in thin films. The role of nitrogen in the capping layer, for preventing melt agglomeration by improved wetting at the molten Si/SiO$_2$ cap interface, is clearly demonstrated in three papers. Laser crystallization of III-V compounds has resulted in polycrystalline materials with grains of a few microns.

Heteroepitaxy usually allows lower processing temperature than the melt and recrystallization approach. Two types of research activities are represented in Part II. With the well established silicon-on–sapphire (SOS) technology, advances are illustrated by the high-performance submicron CMOS circuits fabricated in low-defect (< 0.1% microtwin) SOS films grown by solid phase epitaxy (SPE). With other materials, novel techniques are discussed for growing various combinations of semiconducting films of Si, Ge or III-V compounds with insulating layers of alkaline earth fluorides, boron phosphide, spinel or SiO$_2$. The results presented here reflect significant improvement in crystalline quality and surface morphology for many of these films. Some of the techniques used were amorphization and subsequent SPE, low temperature predeposition, lattice constant matching with mixed-compounds, patterning of underlying layers, laser or rapid thermal annealing, a special gas mixture in epitaxial reactors, and a porous silicon substrate. Si films formed by the predeposition technique on CaF$_2$ have a $x_{min}$ of less than 10%. Working devices, with characteristics approaching those of bulk semiconductor devices, are also reported in several papers. Most noteworthy are the three dimensional circuits with functioning devices in up to four layers of Si/BP.
There were few papers presented at the symposium on porous silicon in the conventional SOI sense. However, a novel derivation of the technique to generate a buried conducting layer in silicon stimulated the imagination of many in the audience.

Part II gives an account of the flourishing activities and dramatic advancements in ion beam synthesized insulators now becoming possible with the availability of high current implanters. There are reports on the use of post O⁺ implantation annealing at unprecedentedly high temperatures (1300–1400°C) to achieve a low-defect SOI overlayer, to annihilate O thermal donors near the top Si surface, and to generate abrupt Si/SiO₂/Si interfaces. These Si overlayers were characterized by a \( x_{\text{min}} \) of 3.3%, and threading dislocation densities of \( 10^6 \) to \( 10^9/cm^2 \). Papers on gettering of heavy metals by implant-damaged regions, and achievement of high quality epitaxial Si grown on oxygen implanted SOI (SIMOX), further suggest the readiness of this material for device and circuit fabrication. Although in its relative infancy, buried nitride requires a lower post implantation annealing temperature (1200–1250°C) to form abrupt interfaces and to generate a Si overlayer of comparable quality \( x_{\text{min}} = 3\% \). Still, problems in void formation, electrical leakage of the buried nitride, and N thermal donor formation remain causes for concern on its practical applications.

Experimental evidence that thermal stress is partly responsible for the formation of subboundaries and the predominance of the <100> texture in ZMR Si is offered by the first paper in Part IV. The following papers discuss application of various structural characterization techniques, including a pulsed laser atom probe for the microscopic Si/SiO₂ interface, a Raman microprobe for local stress, a UV reflectance and ellipsometry study of SOS material, and the use of Seebeck emf for in-situ detection of growth dislocations across the solid/liquid interface. A trio of papers on electrical characterization expound on the advantage of using depletion mode transistors in the current transient mode of deep level transient spectroscopy for their high sensitivity, small sampling area, and versatility in measurement configurations. Minority carrier generation lifetimes have been clearly correlated with such defects as precipitates of impurities, subboundaries or interface states in recrystallized films. Depth profiles of mobility can also be obtained.

One of the major applications of SOI materials is direct replacement of certain critical bulk Si VLSI circuits with those isolated from the Si substrate by a thin insulator. The first paper in Part V very eloquently states the potential advantages of complete dielectric isolation, increased packing density, reduced parasitic capacitance and radiation hardness. High performance MOS and bipolar devices and SSI circuits have been built routinely to characterize the ZMR and SPE material. Fully functioning LSI circuits have also been demonstrated in ZMR Si and SIMOX. However, improvement in material quality and/or innovation in device design are still needed to implement submicron VLSI circuits in SOI.

A case in point is the use of polysilicon transistors in 3-dimensional integrated circuits. The decision to build less critical components in the inferior polysilicon SOI material and the ensuing simplified process greatly facilitated demonstration and commercialization of 64K and 256K VLSI CMOS memories. An even more radical approach to 3-D ICs is the ELVIG (Elemental Level Vertically Integrated Circuit) method. Two IC chips fabricated with two different technologies (for example, NMOS and PMOS) are electrically merged through vertical interconnects by thermal compression bonding. Initial success has been shown in 31-stage ring oscillators. As for 3-D ICs with more than one layer of SOI structures, heteroepitaxy in solid state seems to offer the most promise because of its low processing temperature.
The other major application of SOI materials is building thin film transistors (TFTs) on non-Si substrates for opto-, acousto-, or magneto-electronic input/output devices to achieve parallel data transmission at system interfaces. Examples in this symposium include a silicon-on-garnet material for magnetic bubble memories, an image sensor array, and the flat panel displays referred to by numerous papers throughout the book. Since the substrate often plays an active role in the total system, process compatibility is usually more important than obtaining defect-free SOI material. Indeed, both polysilicon and amorphous silicon are often preferred over recrystallized Si in TFT fabrication because of their low processing temperature and large area deposition capability. The five papers on polysilicon TFTs deal with process optimization, grain boundary passivation, diffusion doping, leakage current control, and device modeling. The final three papers pertaining to amorphous silicon TFTs fabrication, gate dielectrics, and photoluminescence properties provide only a sample of the vast volume of literature on amorphous silicon material and devices. The reader is referred to other recent volumes of MRS Proceedings for more extensive coverage on this subject.

Symposium Chairs
Anne Chiang     Michael W. Geis     Loren Pfeiffer

June 1986
Acknowledgments

We wish to thank all of the contributors and participants who made the symposium so successful. We particularly would like to acknowledge the invited speakers, who provided excellent summaries of specific areas and set the tone of the meeting. They are:

R. H. Baughman  
D. J. Dumin  
T. Enomoto  
J. M. Gibson  
D. W. Greve  
C. R. M. Grovenor  
P. L. F. Hemment  
H. Ishiwar a  

K. A. Jackson  
N. M. Johnson  
H. W. Lam  
H. Shichijo  
H. I. Smith  
B-Y. Tsaur  
P. K. Vasudev  
M. S. Wrighton

We are also indebted to the session chairs, who directed the sessions, guided the discussions, and gave invaluable help in getting the papers refereed. They are:

H. Baumgart  
G. K. Celler  
C. K. Chen  
T. I. Kamins  
S. Malhi  
L. A. Nesbit  

J. M. Phillips  
R. F. Pinizzotto  
F. A. Ponce  
J. A. Roth  
J. C. Sturm

It is our great pleasure to acknowledge, with gratitude, the administrative support from Xerox Corporation, and the financial support provided by the Rome Air Development Center; the Army Research Office, Materials Science Division; and the Naval Research Laboratory.

Finally we wish to express our appreciation to V. Moffat (Xerox), I. Collins (Lincoln Lab), and H. Weston (AT&T Bell Labs) for excellent secretarial support, as well as S. Marsh and N. Geis for expert assistance in putting this book together.