High Performance ASIC Design: Using Synthesizable Domino Logic in an ASIC Flow

Presenting methodologies for high speed ASIC design developed over several years in industry, this practical book covers issues related to the use of domino logic in an automated framework, and brings together all the knowledge needed to apply them in practice.

An overview of design techniques used to achieve high speed in ASIC designs is followed by chapters describing the design and characterization of domino logic standard cell libraries and an advanced domino logic synthesis flow. Actual results achieved by using automated domino logic design techniques, including silicon measurements, are presented to validate the methodology, whilst real-world design examples, such as the implementation of the execution unit of a microprocessor and Viterbi decoder, show how the techniques are applied in practice. This book is ideal for graduate students and researchers in electrical and computer engineering, and also for circuit designers and EDA engineers in industry.

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Preface

This book stems from my experience over the last few years in designing high-speed digital logic using ASIC design flows. I discovered that while it is possible to significantly improve performance in ASIC implementations with deep pipelining and careful physical design, a speed penalty still had to be paid due to their exclusive use of static logic. This spurred an interest in using domino logic with automated synthesis and place and route tools. This book documents my experiences in automating the use of domino logic, and shows that despite the challenges entailed in the process, it is possible to use domino logic with industry-standard ASIC tools and achieve a significant speed improvement in the process.

Engineering is a group activity. The development of our domino logic synthesis system was possible due to the collaboration of many intelligent, enthusiastic, and dedicated co-workers whose contributions I must acknowledge. First of all I would like to thank my two chapter co-authors, Tommy Zounes and Bernard Bourgin. In addition to being gifted and hard-working engineers, Tommy and Bernard have also always been very generous with their knowledge and time, allowing all of their co-workers, including me, to learn a great deal from them. The domino logic library was possible due to the talents and efforts of Scott Anderson, Shaun Forsting, Judy Alvarez-Gallardo, Roger Boates, Michael Lin, and Juneho Park, who helped design the schematics and also contributed to the myriad other tasks involved with taping out a number of chips. Scott, armed with a contagious optimism, also helped me document our early experiences with using domino logic. Shaun Forsting converted the schematics into very efficient layouts across a number of different CMOS processes. During the early years of the domino logic project we were joined by two engineers from Italy: Fabrizio Viglione and Marco Cavalli. They both worked on the first domino chips with great enthusiasm and effectiveness. Fabrizio subsequently took the first stab at implementing our approach to synthesizing domino logic. From France we were later joined by the affable Leonardo Valencia, who with Cyril Adobati and Robin Wilson completed the first design that used a fully synthesizable domino logic flow. Roy Mader and Boris Andreev worked on the project as summer interns. Roy subsequently became a much-valued permanent member of our group and led us in overcoming many of the onerous challenges involved in pushing domino designs through automated place and route flows.

People work effectively only in a supporting environment. I would like to thank our manager Naresh Soni for encouraging and supporting us in our work in domino

synthesis, as well as Joel Monnier, who led STMicroelectronics' Central Research and Development organization. They provided us with the extraordinary luxury of being allowed to innovate in an autonomous manner. Nick Richardson, who later led the group, continued in this fine tradition and also provided more specific technical advice on matters related to logic and architecture. In addition, I must thank the many others in STMicroelectronics who supported us in our work on domino logic, including: Philippe Magarshack, Jean-Pierre Schoellkopf, Sylvain Kritter, Heloise Tupin, Damien Croain, Alain Chion, Samala Sreekiran, Sanjay Bulusu, Ezio Iacazio, and Marco Gregori.

I would like to thank my wonderful parents, Mosharaff and Inari Hossain, who have encouraged me throughout this endeavor, and more broadly, instilled in me a love of books and learning. Finally I must thank my beloved wife, Zakia Chowdhury, whose support allowed me to write this book. I dedicate this book to her and my two delightful sons, Farhan and Ishraq.

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Abbreviations

ASIC	application-specific integrated circuit
CMOS	complementary metal oxide semiconductor
CSA	carry save adder
CTO	clock tree optimization
DRC	design rule check
DSPF	detailed standard parasitic format
DVD	digital video disc
ECO	engineering change order
EDA	electronic design automation
FET	field effect transistor
fF	femtofarad
FO4	fan-out of four
GHz	gigahertz
HDL	hardware description language
LFSR	linear feedback shift register
LSB	least significant bit
LVS	layout versus schematic
MHz	megahertz
MIPS	million instructions per second
MPC	minimum physical constraints
MPWH	minimum pulse width high
MPWHO	minimum pulse width high overlap
MPWL	minimum pulse width low
MSB	most significant bit
MUX	multiplexer
NMOS	n-channel metal oxide semiconductor
PLL	phase locked loop
PMOS	p-channel metal oxide semiconductor
PUT	pin under test
PVT	process, voltage, and temperature
QoR	quality of results
RC	resistor capacitor circuit
RF	radio frequency

RISC	reduced instruction set computer
RTL	register transfer level
SDC	Synopsys design constraints
SOC	system-on-chip
SRAM	static random access memory
TAT	turnaround time
VCO	voltage-controlled oscillator
VLSI	very large scale integration
XNOR	exclusive NOR
XOR	exclusive OR
μm	micrometer