

Index

- 2-D pipelining 129
- 2-way arbiters 33–34
- 4-phase bundled-data 17
- channel 6, 48
 - 1-of-1 20, 22, 32
 - 1-of-N 18–19, 20
 - 1-of-N+1 20, 220
 - 1-of-4 20
 - 1-of-8 20
- abstraction 43
- acyclic network 33
- ack 131
 - signal 107
 - wire 16
- active port 22
- all pairs shortest path algorithm 92
- analog verification 3
- Arbiters 33
- AMULET 154
- ARM996HS 195
- ARM9E 195
- ARM V5T 194
- ASIC 2, 4, 5
- asynchronous
 - architectures 12
 - channels 16
 - controllers 12
 - crossbar 38
 - design 1, 2, 5, 6, 7, 8
- at-speed testing 9
- automatic test pattern generation (ATPG)
 - 190, 192
- average-case
 - delay 8
 - performance 8
- back-end flows 7
- Balsa 46
- bit-bucket 27, 28, 71, 202
- bit-generator 27, 202
- blocks (network of blocks) 16
- Bounded delay design 118
- broad 17
- bubble 70, 110
 - limited region 70, 77, 80
 - shuffling 230
 - starvation 108
- Bundled data 20, 124–125, 152
 - channels 16, 17–18, 21, 152
- bundling constraints 152, 155
- buffer 28
 - insertion 5
- burst-mode 138
- CALL module 157
- C-element 7, 156, 190
 - asymmetric 123, 216
 - Muller 121
- capacity 28
- capture-pass latches 152
- CAST 47
- characterization 3
- charge sharing 122, 333
- choice 85
- clock 1, 2, 3, 4, 5, 7, 8
 - driver 9
 - frequency 66
 - gating 5, 9
 - period 3
 - skew 3, 8
 - tree 5, 8
- combinational 3, 4
 - cycle 7
- Communicating Sequential Processes 172
- concurrency 24, 85
- conditional 30
 - communication 108
- connector 176
- consumed 16
- control kiting 154
- co-simulation 43
- critical path 67
- crossbar 111
- cross-talk 1, 4, 5

- cross-coupling 5
- CSP 43, 44, 45, 52, 129
 - macros 55
- cycle time 66, 87, 89
- D-element 168
- data wires 6
- data
 - dependant data flow 8
 - dependant delay 8
 - driven 22
 - driven decomposition 129
 - limited region 70, 78
- Datapath design 123
- Deadlock 45, 54, 58, 106
- decomposition 6, 7, 129
- deep submicron 4
- demand-driven 22
- delay line 152, 165, 166
 - reset constraint 166
- delay model 116
- delay-insensitive 18–19, 116
- de-synchronization 131
- deterministic system 66
- DETFs 154
- DfT 192
- dining philosophers' problem 45, 106
- distributed noise spectrum 10
- domino logic 7, 8
- dual-rail 9, 19, 20, 184
- dual-ported memories 32
- dynamic
 - cell library 5
 - hazard 142
 - logic 5, 120–121
- early
 - done 242
 - evaluation 242
 - protocol 17
- electromagnetic 7, 10
- enable 20
- enclosed handshake 24
- evaluate transistors 8
- event 100
 - driven 9
 - modules 155
 - rule systems 89
- Euclid's algorithm 74–76
- false wire 20
- flow table 136
- force 55
- four-phase
 - handshaking 177
 - protocol 24, 27
- fork 29, 79, 96, 117
- formal verification 107, 161
- flip-flops (FFs) 2, 3, 5, 9, 29
- flow control 28
- FIFO 28, 36
- free slack 98
- FSM 32
- Fulcrum Microsystems 6
- full buffer 28, 71, 89, 159
 - Channel Net (FBCN) 88, 96
- fully-decoupled handshake protocol 27
- full-custom 2, 3–4, 5, 7, 8
- fundamental mode 119, 136, 138
- FPGA 2
- gate-level netlist 7
- GasP 21
- Globally asynchronous, locally synchronous (GALS) 304
- half buffer 28, 71, 89, 159, 201
- handshaking 5, 6, 11
 - 4-phase 107
 - circuitry 7
 - disciplines 11
 - primitives 7
- Handshake Solutions 7, 11, 12, 172
- handshake channels 173
- Harvard architecture 194
- Haste 11, 47
- HDL 43
- high capacity 28
- hold time 3
- increased variations 1
- Indictability 126–129
- inertial delay model 201
- input completion sensing 217
- INPORT/OUTPORT 48
- input-output mode 119
- isochronic 200
- Isochronic forks 117
- isochronic fork assumption 335
- join 30, 97
- Karp's algorithm 94–95
- KPB based addr 181
- late protocol 17
- latency 66
 - backward 68–69
 - forward 67, 88
- latency-insensitive design 10, 73
- LARD 46
- leaf cells 6, 16, 88, 116

- level
 - encoded two-phase dual-rail (LEDR) 130
 - sensitive latches 9
- linear
 - pipelines 72
 - programming 92
- local cycle time 68
- logical effort 8
- long-term average 66
- loop control 32
- Lookahead Pipelines
 - LP2/1 246
 - LP2/2 244
 - LP3/1 242
 - LPSR2/2 247
 - LPSR2/1 249
 - LPHC 250
- macro cell 6
- master-slave flip-flop 152
- marked
 - graph 241
 - group 203
- maximum cycle mean 90, 94
- MERGE 30
- metastability 278, 304, 308
- micropipeline 12, 152
- middle data-validity protocol 22
- MIPS R3000 194
- module 16
- modularity 9
- MOUSETRAP pipeline 154
- mutual-exclusion element 236
- Mingle input change circuit 137
- multi-rail 9
- N-way arbiter 34
- narrow protocol 17
- Non-linear pipelines 29
- non-deterministic system 66
- non-weak conditioned STFB 272
- noise margin 3, 5
- Null Convention Logic (NCL) 130
- one-ported memory 32
- one-hot state encoding 32
- one-sided timing constraint 118
- PAR module 25
- passive port 22
- peep-hole optimization 7, 172, 187–188
- performance 8, 12, 90
- Petri Nets 84
- pipeline 12
 - arbiters 35
 - handshake 27
 - loops 73
 - template 8
- PLI (Programming Language Interface) 48
- plug-and-play 10
- precharge 8
 - constraint 254
- pre-charged half buffer (PCHB) 204, 289
- pre-charged full buffer (PCFB) 216
- probabilistic timed Petri nets (PTPN) 100
- point-to-point 6, 21
- Phased Logic 130
- Phillips Research 7
- primitives 48
- probe 44
- pseudo-static 120–121
- PS0 pipeline 240
- pull channel 22, 182
- pure delay model 201
- push 16
- pulse generator 270
- quasi-delay-insensitive (QDI) 117, 200
 - design 125–126
- receive 7, 44, 48
- reachability graph 86
- reconvergent
 - paths 6
 - fanouts 118
- reduced
 - broad validity protocol 185
 - electromagnetic interference 10
 - stack pre-charged full buffer (RSPCFB) 229
 - stack RSPCHB 220
- request
 - breakers 227
 - lines 16
- refinement 6
- relative timing 119
- resource sharing 157
- ring 73, 76, 77
- RTL 130
- SAMIPS 194
- select line
 - hold constraint 167
 - setup constraint 166
- setup
 - margin 8
 - time 3
- semi-custom 2, 3, 5, 7
- send 7, 44, 48, 55
- SEQ module 24
- sequencing operations 24
- single
 - input change circuit 137
 - rail 184

- track 20, 28, 267
- track asynchronous pulsed logic (STAPL) 270
- track full-buffer (STFB) 271
- static single-track 269
- simple four-phase protocol 28
- shared asynchronous channel 21
- slack 89
 - elastic 40, 73, 131
 - dynamic 71, 77, 81
 - matching 81, 96, 98
 - slack 71
- slackless 35
- stalled right environment (SRE)
 - problem 254
- SPA 194
- space 110
- SpecC 132
- Speed Independent design 117–118
- SPLIT 30
- stable state 136
- stalled left environment (SLE) problem 255
- standard-cell 7
- starvation 45
- state machine 12, 85
- static
 - hazard 142
 - logic 8, 12, 120
 - timing 3
- staticizer 121
- STG-based 132
- stochastic timed Petri nets (STPN) 100
- stuck-at fault 189
- synchronous
 - cell 7
 - channel 22
 - design 2, 4, 6, 8
 - scan 192
 - worst-cast delay 8
- SystemC 47
- static CMOS 3
- statisizers 20
- syntax
 - directed design 11, 12
 - directed translation 7, 172, 176
 - driven translation 130
- synthesis-based controller 136
- System-on-chip (SoC) 304
- Tangram 46, 47, 172
- testbench 55
- testing 10–11
- timed execution 100
- token 20, 75
 - buffer 33, 234, 283
 - starvation 108
- translating 7
- transferer 26
- tri-state 20
- Theseus Logic 7, 130
- throughput 66, 73
- Timed Marked Graph 88
- time separation of an event pair (TSE) 101
- timed event 101
- timed event graph 101
- timing
 - assumption 6, 19, 118
 - closure 4
 - constraint 5, 118
- TOGGLE 158
- true four phase protocol 187
- true four phase handshaking 162
- T4PFB 163
- true wire 20
- two-phase
 - arbiter 157
 - handshaking 16
 - protocol 16, 24
- two-sided timing constraints 119
- transition signaling 16
- unconditional 30
- useful skew 8
- VAR 30
- Verilog 12, 43
- VerilogCSP 48, 52, 108
- VHDL 43
- VLSI 43
- voltage scaling 9
- wait graph 58
- weak-conditioned
 - half buffer (WCHB) 200, 289
 - logic 201
- wire delay 4
- wire resistance 1