A Designer's Guide to Asynchronous VLSI

Create low power, higher performance circuits with shorter design times using this practical guide to asynchronous design. This practical alternative to conventional synchronous design enables performance close to full-custom designs with design times that approach commercially available ASIC standard cell flows. It includes design trade-offs, specific design examples, and end-of-chapter exercises. Emphasis throughout is placed on practical techniques and real-world applications, making this ideal for circuit design students interested in alternative design styles and system-on-chip circuits, as well as for circuit designers in industry who need new solutions to old problems.

Peter A. Beerel is CEO of TimeLess Design Automation – his own company commercializing asynchronous VLSI tools and libraries – and an Associate Professor in the Electrical Engineering Department at the University of Southern California (USC). Dr. Beerel has 15 years' experience of research and teaching in asynchronous VLSI and has received numerous awards including the VSoE Outstanding Teaching Award in 1997 and the 2008 IEEE Region 6 Outstanding Engineer Award for significantly advancing the application of asynchronous circuits to modern VLSI chips.

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To Janet, Kira, and Kim
– P. A. B.

To Jemelle and Charlotte
– R. O. O.

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