Integrated Frequency Synthesizers for Wireless Systems

The increasingly demanding performance requirements of communications systems, as well as problems posed by the continued scaling of silicon technology, present numerous challenges for the design of frequency synthesizers in modern transceivers.

This book contains everything you need to know for the efficient design of frequency synthesizers for today's communications applications. If you need to optimize performance and minimize design time, you will find this book invaluable.

Using an intuitive yet rigorous approach, the authors describe simple analytical methods for the design of phase-locked loop (PLL) frequency synthesizers using scaled silicon CMOS and bipolar technologies. The entire design process, from system-level specification to layout, is covered comprehensively. Practical design examples are included, and implementation issues are addressed.

A key problem-solving resource for practitioners in integrated-circuit design, the book will also be of interest to researchers and graduate students in electrical engineering.

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CAMBRIDGE UNIVERSITY PRESS

CAMBRIDGE UNIVERSITY PRESS
Cambridge, New York, Melbourne, Madrid, Cape Town, Singapore, São Paulo

Cambridge University Press
The Edinburgh Building, Cambridge CB2 8RU, UK

Published in the United States of America by Cambridge University Press, New York

www.cambridge.org
Information on this title: www.cambridge.org/9780521863155

First published 2007

Printed in the United Kingdom at the University Press, Cambridge

A catalogue record for this publication is available from the British Library

ISBN 978-0-521-86315-5 hardback

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Preface

The phase-locked loop (PLL) concept is about 70 years old and a wealth of literature is already available on the subject. Someone may therefore ask why another book about PLLs.

The first reason is related to the specific application considered here, namely the silicon integration of frequency synthesizers. Classical texts do not deal in depth with issues related to the design of frequency synthesizers in modern transceivers. In particular, the design guidelines and the performance of some important building blocks and their impact on the whole system are sometimes barely mentioned. The attempt, here, has been instead to provide a broad description of the most typical circuit topologies of voltage-controlled oscillators, frequency dividers and phase and frequency detectors, and to discuss their performance in terms of power consumption, phase noise, spurs, and so forth. A chapter is also devoted to integrated passive components, such as varactors and inductors, since the ability to optimize their performance judiciously is becoming a key skill required of the RF designer.

The second reason is that the book attempts to provide an alternative approach to PLL theory and design. After years of research and study on the subject, the authors propose an analysis methodology that is both rigorous and intuitive. The ability to simplify the picture and to address schematically the impact of complex, often non-linear, effects is a fundamental skill of any good engineer. The PLL is a good training example for the designer. In this respect, the book provides many examples of models, starting from a schematic and simplified description of the circuit operation and then leading to estimates, which are compared with simulation results. These examples are intended not only to provide a deeper insight into complex and intriguing effects, but also to encourage students and young analogue designers to keep exercising the ability to figure out the consequences of technical choices before performing circuit simulations.

The book starts with three chapters addressing the PLL as a system. Chapter 1 points out the typical requirements of the frequency synthesizer in RF systems. Chapter 2 covers some PLL basics. It does not deal with the whole PLL theory, which is analyzed in depth in many classical books. The chapter highlights only the concepts needed for understanding the subsequent topics. Chapter 3 finally analyzes fractional-division PLLs, which are seldom discussed in other texts.

Chapters 4 to 9 are then devoted to discussing in detail the design issues related to the PLL building blocks. Chapters 4 to 7 deal with voltage-controlled oscillators and their practical implementations in bipolar and CMOS technologies, including resonator design and layout. Chapters 8 and 9 are focused on the design of programmable dividers and phase-comparison circuits, including issues related to non-linearities.

Acknowledgments

The research activity behind this book has been in progress for more than ten years. It was made possible thanks to the financial support provided by the Italian Ministry of Universities and Research and by industry. In this respect, many thanks go to Mario Paparo of STMicroelectronics (Catania, Italy), Maurizio Pagani of Ericsson Lab (Vimodrone, Italy), and to Mihai Banu of the (formerly) Silicon Circuit Research Department of Bell Laboratories (Murray Hill, NJ), for their strong support.

The authors are indebted to all their past graduate students, Mr Francesco Villa, Dr Alfio Zanchi, Dr Andrea Bonfanti, Dr Luca Romanò, Dr Stefano Pellerano, Dr Marco Milani and Dr Luigi Panseri, who shared the excitements of this research and contributed to most of the understanding reported in the following pages. The authors are also extremely grateful to their current Ph.D. students, Paolo Madoglio and Marco Zanuso, who worked out the examples and the simulations, providing critical revisions of the text. Clearly, only the authors are responsible for any errors that may still be present.