

Contents

<i>Preface</i>	<i>page xi</i>
Part 1 Preliminaries	
1 Number systems and codes	3
1.1 Number systems	3
1.2 Binary codes	10
1.3 Error detection and correction	13
Notes and references	19
Problems	20
2 Sets, relations, and lattices	23
2.1 Sets	23
2.2 Relations	25
2.3 Partially ordered sets	28
2.4 Lattices	30
Notes and references	33
Problems	33
Part 2 Combinational logic	
3 Switching algebra and its applications	37
3.1 Switching algebra	37
3.2 Switching functions	44
3.3 Isomorphic systems	52
3.4 Electronic-gate networks	57
*3.5 Boolean algebras	58
Notes and references	60
Problems	61

vi	Contents	
	4 Minimization of switching functions	67
	4.1 Introduction	67
	4.2 The map method	68
	4.3 Minimal functions and their properties	78
	4.4 The tabulation procedure for the determination of prime implicants	81
	4.5 The prime implicant chart	86
	4.6 Map-entered variables	93
	4.7 Heuristic two-level circuit minimization	95
	4.8 Multi-output two-level circuit minimization	97
	Notes and references	100
	Problems	101
	5 Logic design	108
	5.1 Design with basic logic gates	108
	5.2 Logic design with integrated circuits	112
	5.3 NAND and NOR circuits	125
	5.4 Design of high-speed adders	128
	5.5 Metal-oxide semiconductor (MOS) transistors and gates	132
	5.6 Analysis and synthesis of MOS networks	135
	Notes and references	143
	Problems	144
	6 Multi-level logic synthesis	151
	6.1 Technology-independent synthesis	151
	6.2 Technology mapping	162
	Notes and references	169
	Problems	170
	7 Threshold logic for nanotechnologies	173
	7.1 Introductory concepts	173
	7.2 Synthesis of threshold networks	181
	Notes and references	200
	Problems	202
	8 Testing of combinational circuits	206
	8.1 Fault models	206
	8.2 Structural testing	212
	8.3 I_{DDQ} testing	220
	8.4 Delay fault testing	224
	8.5 Synthesis for testability	232
	8.6 Testing for nanotechnologies	250
	Notes and references	254
	Problems	257

Part 3 Finite-state machines

9 Introduction to synchronous sequential circuits and iterative networks	265
9.1 Sequential circuits – introductory example	265
9.2 The finite-state model – basic definitions	269
9.3 Memory elements and their excitation functions	272
9.4 Synthesis of synchronous sequential circuits	280
9.5 An example of a computing machine	293
9.6 Iterative networks	296
Notes and references	300
Problems	300
10 Capabilities, minimization, and transformation of sequential machines	307
10.1 The finite-state model – further definitions	307
10.2 Capabilities and limitations of finite-state machines	309
10.3 State equivalence and machine minimization	311
10.4 Simplification of incompletely specified machines	317
Notes and references	330
Problems	330
11 Asynchronous sequential circuits	338
11.1 Modes of operation	338
11.2 Hazards	339
11.3 Synthesis of SIC fundamental-mode circuits	346
11.4 Synthesis of burst-mode circuits	358
Notes and references	363
Problems	365
12 Structure of sequential machines	372
12.1 Introductory example	372
12.2 State assignments using partitions	375
12.3 The lattice of closed partitions	380
12.4 Reduction of the output dependency	383
12.5 Input independency and autonomous clocks	386
12.6 Covers, and the generation of closed partitions by state splitting	388
12.7 Information flow in sequential machines	395
12.8 Decomposition	404
*12.9 Synthesis of multiple machines	413
Notes and references	418
Problems	419

13 State-identification experiments and testing of sequential circuits	431
13.1 Experiments	431
13.2 Homing experiments	435
13.3 Distinguishing experiments	439
13.4 Machine identification	440
13.5 Checking experiments	442
*13.6 Design of diagnosable machines	448
13.7 Alternative approaches to the testing of sequential circuits	453
13.8 Design for testability	458
13.9 Built-in self-test (BIST)	461
Appendix 13.1 Bounds on the length of synchronizing sequences	464
Appendix 13.2 A bound on the length of distinguishing sequences	467
Notes and references	467
Problems	468
14 Memory, definiteness, and information losslessness of finite automata	478
14.1 Memory span with respect to input–output sequences (finite-memory machines)	478
14.2 Memory span with respect to input sequences (definite machines)	483
14.3 Memory span with respect to output sequences	488
14.4 Information-lossless machines	491
*14.5 Synchronizable and uniquely decipherable codes	504
Appendix 14.1 The least upper bound for information losslessness of finite order	510
Notes and references	512
Problems	513
15 Linear sequential machines	523
15.1 Introduction	523
15.2 Inert linear machines	525
15.3 Inert linear machines and rational transfer functions	532
15.4 The general model	537
15.5 Reduction of linear machines	541
15.6 Identification of linear machines	550
15.7 Application of linear machines to error correction	556
Appendix 15.1 Basic properties of finite fields	559
Appendix 15.2 The Euclidean algorithm	561
Notes and references	562
Problems	563
16 Finite-state recognizers	570
16.1 Deterministic recognizers	570
16.2 Transition graphs	572

16.3	Converting nondeterministic into deterministic graphs	574
16.4	Regular expressions	577
16.5	Transition graphs recognizing regular sets	582
16.6	Regular sets corresponding to transition graphs	588
*16.7	Two-way recognizers	595
	Notes and references	601
	Problems	602
	<i>Index</i>	608