Switching and Finite Automata Theory

Understand the structure, behavior, and limitations of logic machines with this thoroughly updated third edition.

New topics include:
- CMOS gates
- logic synthesis
- logic design for emerging nanotechnologies
- digital system testing
- asynchronous circuit design

The intuitive examples and minimal formalism of the previous edition are retained, giving students a text that is logical and easy to follow, yet rigorous. Kohavi and Jha begin with the basics, and then cover combinational logic design and testing, before moving on to more advanced topics in finite-state machine design and testing. The theory is made easier to understand with 200 illustrative examples, and students can test their understanding with over 350 end-of-chapter review questions.

Zvi Kohavi is Executive Vice President and Director General at Technion–Israel Institute of Technology. He is Professor Emeritus of the Computer Science Department at Technion, where he held the position of Sir Michael and Lady Sobell Chair in Computer Engineering and Electronics.

Niraj K. Jha is a Professor at Princeton University and a Fellow of the IEEE and ACM. He is a recipient of the AT&T Foundation Award and NEC Preceptorship Award for research excellence, the NCR Award for teaching excellence, and Princeton’s Graduate Mentoring Award.
Switching and Finite Automata Theory

Third Edition

Zvi Kohavi
Technion–Israel Institute of Technology

Niraj K. Jha
Princeton University
## Contents

**Preface**  
page xi

**Part 1 Preliminaries**

1 Number systems and codes  
1.1 Number systems 3  
1.2 Binary codes 10  
1.3 Error detection and correction  
 Notes and references 19  
 Problems 20

2 Sets, relations, and lattices 23  
2.1 Sets 23  
2.2 Relations 25  
2.3 Partially ordered sets 28  
2.4 Lattices 30  
 Notes and references 33  
 Problems 33

**Part 2 Combinational logic**

3 Switching algebra and its applications 37  
3.1 Switching algebra 37  
3.2 Switching functions 44  
3.3 Isomorphic systems 52  
3.4 Electronic-gate networks 57  
*3.5 Boolean algebras 58  
 Notes and references 60  
 Problems 61

© in this web service Cambridge University Press  
www.cambridge.org
# Contents

## 4 Minimization of switching functions

4.1 Introduction 67  
4.2 The map method 68  
4.3 Minimal functions and their properties 78  
4.4 The tabulation procedure for the determination of prime implicants 81  
4.5 The prime implicant chart 86  
4.6 Map-entered variables 93  
4.7 Heuristic two-level circuit minimization 95  
4.8 Multi-output two-level circuit minimization 97  
Notes and references 100  
Problems 101  

## 5 Logic design

5.1 Design with basic logic gates 108  
5.2 Logic design with integrated circuits 112  
5.3 NAND and NOR circuits 125  
5.4 Design of high-speed adders 128  
5.5 Metal-oxide semiconductor (MOS) transistors and gates 132  
5.6 Analysis and synthesis of MOS networks 135  
Notes and references 143  
Problems 144  

## 6 Multi-level logic synthesis

6.1 Technology-independent synthesis 151  
6.2 Technology mapping 162  
Notes and references 169  
Problems 170  

## 7 Threshold logic for nanotechnologies

7.1 Introductory concepts 173  
7.2 Synthesis of threshold networks 181  
Notes and references 200  
Problems 202  

## 8 Testing of combinational circuits

8.1 Fault models 206  
8.2 Structural testing 212  
8.3 IDQ testing 220  
8.4 Delay fault testing 224  
8.5 Synthesis for testability 232  
8.6 Testing for nanotechnologies 250  
Notes and references 254  
Problems 257
### Part 3  Finite-state machines

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>9  Introduction to synchronous sequential circuits and iterative networks</td>
<td>265</td>
</tr>
<tr>
<td>9.1 Sequential circuits – introductory example</td>
<td>265</td>
</tr>
<tr>
<td>9.2 The finite-state model – basic definitions</td>
<td>269</td>
</tr>
<tr>
<td>9.3 Memory elements and their excitation functions</td>
<td>272</td>
</tr>
<tr>
<td>9.4 Synthesis of synchronous sequential circuits</td>
<td>280</td>
</tr>
<tr>
<td>9.5 An example of a computing machine</td>
<td>293</td>
</tr>
<tr>
<td>9.6 Iterative networks</td>
<td>296</td>
</tr>
<tr>
<td>Notes and references</td>
<td>300</td>
</tr>
<tr>
<td>Problems</td>
<td>300</td>
</tr>
</tbody>
</table>

| 10 Capabilities, minimization, and transformation of sequential machines | 307  |
| 10.1 The finite-state model – further definitions                      | 307  |
| 10.2 Capabilities and limitations of finite-state machines             | 309  |
| 10.3 State equivalence and machine minimization                        | 311  |
| 10.4 Simplification of incompletely specified machines                  | 317  |
| Notes and references                                                  | 330  |
| Problems                                                               | 330  |

| 11 Asynchronous sequential circuits                                    | 338  |
| 11.1 Modes of operation                                                | 338  |
| 11.2 Hazards                                                           | 339  |
| 11.3 Synthesis of SIC fundamental-mode circuits                        | 346  |
| 11.4 Synthesis of burst-mode circuits                                  | 358  |
| Notes and references                                                  | 363  |
| Problems                                                               | 365  |

| 12 Structure of sequential machines                                   | 372  |
| 12.1 Introductory example                                              | 372  |
| 12.2 State assignments using partitions                               | 375  |
| 12.3 The lattice of closed partitions                                 | 380  |
| 12.4 Reduction of the output dependency                               | 383  |
| 12.5 Input independency and autonomous clocks                         | 386  |
| 12.6 Covers, and the generation of closed partitions by state splitting| 388  |
| 12.7 Information flow in sequential machines                          | 395  |
| 12.8 Decomposition                                                    | 404  |
| *12.9 Synthesis of multiple machines                                  | 413  |
| Notes and references                                                  | 418  |
| Problems                                                               | 419  |
## Contents

13 State-identification experiments and testing of sequential circuits 431
  13.1 Experiments 431
  13.2 Homing experiments 435
  13.3 Distinguishing experiments 439
  13.4 Machine identification 440
  13.5 Checking experiments 442
  *13.6 Design of diagnosable machines 448
  13.7 Alternative approaches to the testing of sequential circuits 453
  13.8 Design for testability 458
  13.9 Built-in self-test (BIST) 461
  Appendix 13.1 Bounds on the length of synchronizing sequences 464
  Appendix 13.2 A bound on the length of distinguishing sequences 467
  Notes and references 467
  Problems 468

14 Memory, definiteness, and information losslessness of finite automata 478
  14.1 Memory span with respect to input–output sequences (finite-memory machines) 478
  14.2 Memory span with respect to input sequences (definite machines) 483
  14.3 Memory span with respect to output sequences 488
  14.4 Information-lossless machines 491
  *14.5 Synchronizable and uniquely decipherable codes 504
    Appendix 14.1 The least upper bound for information losslessness of finite order 510
    Notes and references 512
    Problems 513

15 Linear sequential machines 523
  15.1 Introduction 523
  15.2 Inert linear machines 525
  15.3 Inert linear machines and rational transfer functions 532
  15.4 The general model 537
  15.5 Reduction of linear machines 541
  15.6 Identification of linear machines 550
  15.7 Application of linear machines to error correction
    Appendix 15.1 Basic properties of finite fields 559
    Appendix 15.2 The Euclidean algorithm 561
    Notes and references 562
    Problems 563

16 Finite-state recognizers 570
  16.1 Deterministic recognizers 570
  16.2 Transition graphs 572
## Contents

16.3 Converting nondeterministic into deterministic graphs 574  
16.4 Regular expressions 577  
16.5 Transition graphs recognizing regular sets 582  
16.6 Regular sets corresponding to transition graphs 588  
*16.7 Two-way recognizers 595  
Notes and references 601  
Problems 602  

Index 608
Preface

Topics in switching and finite automata theory have been an important part of the curriculum in electrical engineering and computer science departments for several decades. The third edition of this book builds on the comprehensive foundation provided by the second edition and adds: significant new material in the areas of CMOS logic; modern two-level and multi-level logic synthesis methods; logic design for emerging nanotechnologies; test generation, design for testability and built-in self-test for combinational and sequential circuits; modern asynchronous circuit synthesis techniques; etc. We have attempted to maintain the comprehensive nature of the earlier edition in providing readers with an understanding of the structure, behavior, and limitations of logical machines. At the same time, we have provided an up-to-date context in which the presented techniques can find use in a variety of applications. We start with introductory material and build up to more advanced topics. Thus, the technical background assumed on the part of the reader is minimal.

This edition maintains the style of the previous edition in providing a logical and rigorous discussion of various topics with minimal formalism. Thus, theorems and algorithms are preceded by several intuitive examples to ease understanding. The original references for various topics are provided. Of course, readers who want to dig deeper into a subject would need to consult later works also.

The book is divided into three parts. The first part consists of Chapters 1 and 2. It provides introductory background. The second part consists of Chapters 3 through 8. It deals with combinational logic. The third part consists of Chapters 9 through 16. It is concerned with finite automata. Several chapters contain specific topics that are not prerequisites for subsequent chapters, e.g. Chapters 6, 7, 11–16. Such chapters can be selected at the preference of instructors. Sections marked with a star may be omitted without loss of continuity.

The book can be used for courses at the junior or senior levels in electrical engineering and computer science departments as well as at the beginning graduate level. It is intended as a text for a two-semester sequence. The first semester can be devoted to switching theory (Chapters 1, 3–11) and the second
semester to finite automata theory (Chapters 2, 12–16). Other partitions into two semesters are also possible, keeping in mind that Chapters 3–5 are prerequisites for the rest of the book and Chapters 9 and 10 are prerequisites for Chapters 12–16.

Some chapters have undergone major revision and others only minor revision. Two sections have been added to Chapter 4, on heuristic and multi-output two-level circuit minimization. A section has been added to Chapter 5 on CMOS circuit realizations. Chapter 6 has been completely rewritten with an emphasis on technology-independent multi-level logic synthesis as well as on technology mapping. Chapter 7 has been updated with synthesis techniques geared towards emerging nanotechnologies that can efficiently implement threshold, majority, and minority logic. Chapter 8 has also been completely rewritten to include a discussion of fault models, structural testing, \textit{I}DDQ testing, delay fault testing, synthesis for testability, and testing for nanotechnologies. All these topics provide the underpinning for the testing of modern integrated circuits. Minor changes have been made to the flip-flop section in Chapter 9. Chapter 11 has been updated with material on the synthesis of asynchronous circuits that allow multiple input changes, including burst-mode circuits. The substantial revisions of Chapter 13 include the addition of material on sequential test generation, design for testability, and built-in self-test. These concepts are also important for understanding how modern integrated circuits are tested. The problem sets have been expanded in all the above chapters.

The previous edition has been used at many universities, which encouraged us to undertake the task of revising the book. We are grateful for the feedback and comments from Professors Sudhakar Reddy, Israel Koren, and Robert Dick. We are also indebted to students and colleagues at Technion and at Princeton University for providing a stimulating environment that made this revision possible.

Last, but not the least, Niraj would like to thank his father, Dr Chintamani Jha, and his wife, Shubha, without whose encouragement and understanding this edition would not have been possible.

Zvi Kohavi
Niraj K. Jha