LOW-VOLTAGE CMOS RF FREQUENCY SYNTHESIZERS

A frequency synthesizer is one of the most critical building blocks in any wireless transceiver system. Its design is getting more and more challenging as the demand for low-voltage low-power high-frequency wireless systems continuously grows. As the supply voltage is decreased, many existing design techniques are no longer applicable. This book provides the reader with architectures and design techniques that enable CMOS frequency synthesizers to operate at low supply voltages, at high frequencies with good phase noise and with low power consumption. In addition to updating the reader on many of these techniques in depth, this book will also introduce useful guidelines and step-by-step procedures on behaviour simulations of frequency synthesizers. Finally, three successfully demonstrated CMOS synthesizer prototypes with detailed design consideration and description will be presented to illustrate potential applications of the architectures and design techniques described. The book is intended for engineers, managers and researchers who are working or interested in radio-frequency integrated-circuit design for wireless applications.

Howard C. Luong is an associate professor at the Hong Kong University of Science and Technology. He has published over 50 conference and journal papers on low-voltage wireless transceivers and synthesizer designs. He holds two US patents and has five pending. He is a co-author of *Design of Low-Voltage CMOS Switched-Opamp Switched-Capacitor Systems* published by Kluwer Academic Publishers in 2003.

Gerry C. T. Leung was a research assistant at the Hong Kong University of Science and Technology. He is currently working as an RFIC designer at Innovative Systems Corporated, Hong Kong.

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HOWARD CAM LUONG AND GERRY CHI TAK LEUNG
Department of Electrical and Electronic Engineering
Hong Kong University of Science and Technology

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Preface

A frequency synthesizer is one of the most critical building blocks in any integrated wireless transceiver system. Its design is getting more and more challenging as the demand for low-voltage low-power high-frequency wireless systems is continuously increased. At the same time, CMOS processes have advanced and been shown to be more and more attractive due to their potential in achieving systems with the highest integration level and the lowest cost. On the other hand, as the supply voltage is lowered, many existing design techniques for integrated frequency synthesizers are no longer applicable. However, it is still desirable to design RF frequency synthesizers at low supply voltages not only because of the device reliability due to the technology scaling but also because of the integration and compatibility with digital circuits.

There are currently only a few books available on integrated RF CMOS frequency synthesizers. The most comprehensive book on integrated CMOS frequency synthesizers available today is entitled *Wireless CMOS Frequency Synthesizer Design* by Craninckx and Steyaert (1998). More recently, another book entitled *Multi-GHz Frequency Synthesis and Division* by Rategh and Lee was also published in 2001. While the two books are still quite useful, they focus only on advanced design techniques of some selected building blocks, including voltage-controlled oscillators, dividers, and synthesizers, with emphasis only on a particular architecture. There exist many new synthesizer architectures and design techniques that are not covered in detail.

This book is intended to supplement the two books with more comprehensive and in-depth descriptions of building blocks and synthesizer systems, in particular for applications with low supply voltages and high frequencies. Special emphasis is placed on consideration, comparison, trade-offs, and optimization for different design choices. In addition, useful guidelines and step-by-step procedures on behavior simulations of frequency synthesizers will be introduced. Finally, several chip prototypes that were successfully designed and demonstrated at low supply voltages will be described in detail to illustrate potential applications of the architectures and the design techniques presented.

The first prototype demonstrates a fully integrated dual-loop synthesizer for 900 MHz GSM transceivers in a standard 0.5 μm CMOS process with a supply voltage of 2 V and threshold voltages around 1 V. For fair comparison, the second chip prototype employs fractional-*N* synthesizer architecture with sigma–delta modulation for the same GSM system using the same 0.5 μm CMOS process but with a supply voltage of 1.5 V. The third prototype focuses on a monolithic 1 V, 5.2 GHz integer-*N* synthesizer for the WLAN 802.11a transceiver system in a 0.18 μm CMOS process with threshold voltages around 0.5 V. While the first two GSM synthesizers need to cover a frequency band of 25 MHz with a channel spacing of 200 kHz around 900 MHz, the third WLAN synthesizer requires a frequency band of 200 MHz with a channel spacing of 20 MHz around 5.2 GHz.

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