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Introduction

1.1. Motivation

Modern transceivers for wireless communication consist of many building blocks, including low-noise amplifiers, mixers, frequency synthesizers, filters, variable-gain amplifiers, power amplifiers, and even digital signal processing (DSP) chips. Each of these building blocks has a different specification, imposes different constraints, and requires different design considerations and optimization. As a result, wireless transceivers have been exclusively implemented using hybrid technologies, mainly GaAs for low noise and high speed, bipolar for high power, passive devices for high selectivity and CMOS for DSP at the baseband. While taking advantage of the best in each technology, this hybrid combination unfortunately requires multi-chip modules and off-chip components, which not only are costly and bulky, but also consume a lot of power.

However, recent development and advance scaling of deep-submicron CMOS technologies have made it more feasible and more promising to implement a single-chip CMOS wireless transceiver. This single-chip integration is particularly attractive for its potential in achieving the highest possible level of integration and the best performance in terms of cost, size, weight, and power consumption.

Among the many design issues and considerations in single-chip CMOS integration is the aggressive scaling of the channel length. According to the Semiconductor Industry Association's roadmap in November 2001, the channel length will be scaled to be as small as 65 nm in 2007, as illustrated in Fig. 1.1. Such a small channel length is necessary to increase operation frequency and to reduce chip area but, at the same time, inevitably requires low supply voltages to avoid oxide breakdown. Even though the threshold voltages of CMOS devices would also be reduced, they are not scaled in the same proportion as the channel length and the supply voltage because of the leakage current in digital circuits. Moreover, the dynamic power of digital circuits is quadratically proportional to their supply voltages. Consequently,

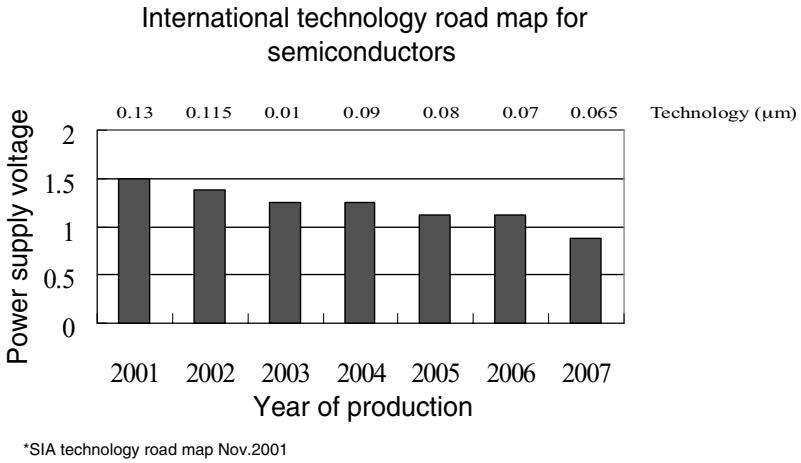

Fig. 1.1 Semiconductor Industry Association's roadmap

the supply voltages for digital circuits have been continuously and aggressively lowered to save power and to extend battery life. To maintain compatibility with the digital parts in wireless transceiver systems, it is necessary that the analog part is designed to operate at the same low supply voltage. Unfortunately, unlike for the digital counterpart, such a low-voltage constraint unavoidably and significantly degrades the performance of analog circuits and, thus, of the whole system, unless novel analog circuit design techniques are developed to compensate and to maintain the same performance.

On-chip voltage multipliers and DC-to-DC boost converters have been proposed to increase the low supply voltage for digital circuits to a higher voltage level in order to power analog circuits and maintain the same performance (Dehng *et al.*, 2000). However, such voltage converters occupy a large chip area, consume extra power, and contribute switching noise to the system. This is the main reason why novel analog design techniques that are suitable for implementation with low supply voltages have become more and more attractive and popular.

It is worth emphasizing that for analog integrated circuits, low-voltage designs do not necessarily result in low power. As a matter of fact, as the supply voltage is lowered, the current consumption typically needs to be increased to maintain the same performance, which in the end can result in even larger total power consumption. In other words, it is always desirable to achieve low power by going to a low supply voltage, but low power should not be the main reason for low-voltage designs. Device reliability due to technology scaling and compatibility with digital circuits in mixed-signal systems should be the main considerations.

One of the greatest challenges to integrating low-voltage single-chip CMOS transceiver systems is to design fully integrated frequency synthesizers for frequency translation and channel selection. First of all, due to very narrow channel spacing, the output signal of the synthesizers needs to be extremely stable and accurate. As a consequence, the phase noise and the spurious performance should be very good. Moreover, the synthesizer's output needs to oscillate at a very high frequency with a sufficiently wide frequency tuning range to cover the whole frequency band and, at the same time, to compensate for any frequency deviation due to process variation. Finally, all these stringent specifications need to be met with limited power consumption and small chip area.

There are several different types of synthesizer architecture, including direct analog synthesis, direct digital synthesizers (DDS) and phase-locked loop (PLL)-based synthesizers (Goldberg, 1996; Yamagishi *et al.*, 1998). Among them, the PLL-based synthesizer is generally most suitable for radio-frequency applications and in general consumes less power consumption with a smaller chip area.

The focus of this book is on design techniques for low-voltage RF CMOS PLL-based frequency synthesizers for wireless transceiver systems. Roughly, low voltage refers to any supply voltage of around 40% to 60% of the maximum allowed supply voltage for a particular process while not exceeding two or three times the threshold voltages of the devices. As examples, in a 0.35 μm CMOS process with a maximum supply of 3.3 V and a threshold voltage of around 0.75 V, a design with a supply voltage of around 1.5 V to 2.0 V is considered a low-voltage design. Similarly, the emphasis is on 1 V designs in 0.18 μm CMOS processes with a maximum supply voltage of 1.8 V and a threshold voltage of around 0.5 V.

1.2. Book organization

The organization of the book is as follows. In Chapter 2 PLL fundamentals and different PLL-based synthesizers will be reviewed together with some brief and qualitative comparison. Chapter 3 will discuss the design issues of the required building blocks and components of PLL synthesizers, including voltage-controlled oscillators, dividers, programmable prescalers, phase frequency detectors, charge pumps, loop-filters, on-chip inductors, varactors, and switched-capacitors arrays. In Chapter 4, guidelines and step-by-step procedures to perform behavioral modeling and simulations of PLL will be presented. Chapter 5 addresses, and elaborates on, special design issues and techniques suitable for high-frequency low-power integrated synthesizers at low supply voltages. As a demonstration of potential applications of the system architectures and design techniques discussed, Chapters 6, 7 and 8 will present detailed design considerations, practical issues,

and the successful implementation of several state-of-the-art frequency synthesizers: namely a 2 V dual-loop frequency synthesizer, a 1.5 V 900 MHz fractional-*N* synthesizer with sigma–delta modulation, and a 1 V 5.2 GHz integer-*N* synthesizer in 0.5 μm, 0.5 μm and 0.18 μm CMOS processes, respectively. Finally, conclusions are drawn in Chapter 9.

2

Synthesizer fundamentals

2.1. Introduction

Nowadays, many integrated circuits are operated in the multi-gigahertz range to increase their processing power and data bandwidth. High-speed clock generation is necessary for both RF systems and microprocessor systems. For high-frequency synchronous systems, the clock fluctuation needs to be minimized to prevent race conditions, to shorten the setup time and hold time requirements, and to increase the maximum possible operating speed of clocked systems.

Local oscillators (LOs), key elements in transceivers, are required to down-convert or up-convert RF signals while minimizing degradation of the signal-to-noise ratio (SNR). The LO signal is expected to be an ideal tone, which should be stable and clean and appear as a sharp impulse. Unfortunately, in practical situations, intrinsic noise from devices and noise from the surrounding environment make the LO signal fluctuate. As a result, the LO signal appears with sideband noise as a skirt centered around the impulse in the frequency domain. For wireless applications, this noise performance affects the SNR and is characterized by measuring the phase noise, which is defined as the ratio of the power of the signal at the desired frequency to the power of the signal at an offset frequency. For clocked system applications, jitter is normally used to characterize timing uncertainty of a clock signal in the time domain, which is defined as the deviation of the zero-crossing points from the ideal waveform.

In order to generate a high frequency and stable clock signal, frequency synthesis is necessary. Among many choices, frequency synthesizers using a phase-locked loop (PLL) are the most popular, in particular for high-frequency and low-power signal generation. Basically, a PLL-based synthesizer is a feedback system used to generate a stable clock signal based on a reference signal. The performance of the synthesizer depends heavily on the purity of the reference signal. As a

result, crystals are commonly used to generate the reference frequency in most PLL systems because of their excellent purity and stability.

The first sections of this chapter review noise sources, which contribute to degradation of phase noise, and fundamental concepts. The trade-offs between design parameters in PLL-based synthesizers are also discussed. The second part of the chapter will briefly describe and compare different architectures to implement high-frequency PLL synthesizers.

2.2. Timing jitter

Timing jitter is a statistically measured parameter with a zero-mean Gaussian distribution and is used to characterize the noise performance of clock signals in the time domain. Deviations of the zero-crossing of the rising clock edge or falling clock edge from their ideal positions are quantified by jitter. Long-term jitter, or absolute jitter, $\sigma_{\Delta T}$, can be used to measure the jitter performance of an oscillator and it is expressed as

$$\sigma_{\Delta T} = \sum_{n=1}^{N} (T_n - \bar{T}), \tag{2.1}$$

where T_n is the period of the oscillator output at the nth cycle and $\bar{T}$ is the mean oscillation period (Herzel and Rajavi, 1999). Owing to the existence of flicker noise in CMOS oscillators, the standard deviation of jitter of free running Voltage-controlled Oscillators (VCOs) is proportional to the square root of the measured time before $t_{1/f}$, and directly proportional to the measured time after $t_{1/f}$, where $t_{1/f}$ is the measured time associated with the $1/f$ noise of devices in oscillators. The timing jitter of a free-running oscillator, $\sigma(t)$, is described in Equation (2.2) (Hajimiri, Limotyrakis and Lee, 1999):

$$\sigma(t) = c\sqrt{t} + kt, \tag{2.2}$$

where c and k are constants with and without $1/f$ noise, respectively.

Large jitter will degrade the accuracy of clocked systems for synchronized operations and cause intercommunication errors between systems. A high-performance clocked system requires stringent clock stability. An unstable clock may limit the maximum possible speed of clocked systems and may even cause incorrect data sampling. Thermal noise in devices can cause phase noise and amplitude noise as depicted in Fig. 2.1.

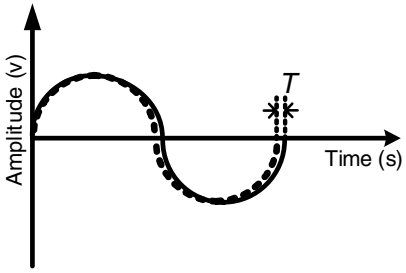

Fig. 2.1 Clock with timing jitter

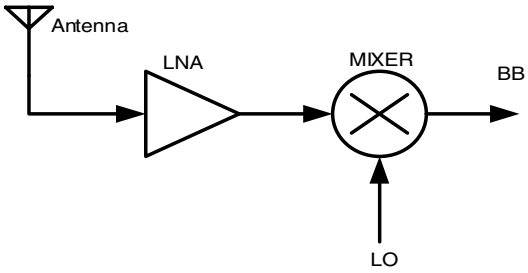

Fig. 2.2 Receiver with LO signal

2.3. Phase noise

Phase noise is defined as the ratio between the total carrier power and the noise power at a frequency offset from the carrier, Δf, which is shown in Equation (2.3).

$$L(\Delta f) = 10 \log \left(\frac{\text{power in 1 Hz bandwidth at } f_0 + \Delta f \text{ frequency offset from carrier}}{\text{total carrier power}} \right), \tag{2.3}$$

where $L(\Delta f)$ is the phase noise in units of decibels per hertz (dBc/Hz), and f_0 is the center frequency of the oscillator.

The higher the required SNR of an RF system is, the better the phase noise for an oscillator is expected. For the receiver in Fig. 2.2, if the LO signal exhibits a non-ideal phase noise as shown in Fig. 2.3, both the desired RF signal and the interference can be simultaneously mixed down by the LO signal. After mixing the interferer can fall directly in the same band as that of the desired signal. Consequently, the SNR is unavoidably degraded. This effect is generally referred to as reciprocal mixing. Since the interference signals are typically much larger than the desired RF signal, the SNR may be unacceptably small unless the phase noise of the LO signal is sufficiently low.

Amplitude noise and phase noise exist in any oscillator. Owing to amplitude limitation in the practical oscillator, phase noise is more severe than amplitude noise (Hajimiri, Limotyrakis and Lee, 1999). Any phase error that occurs in earlier

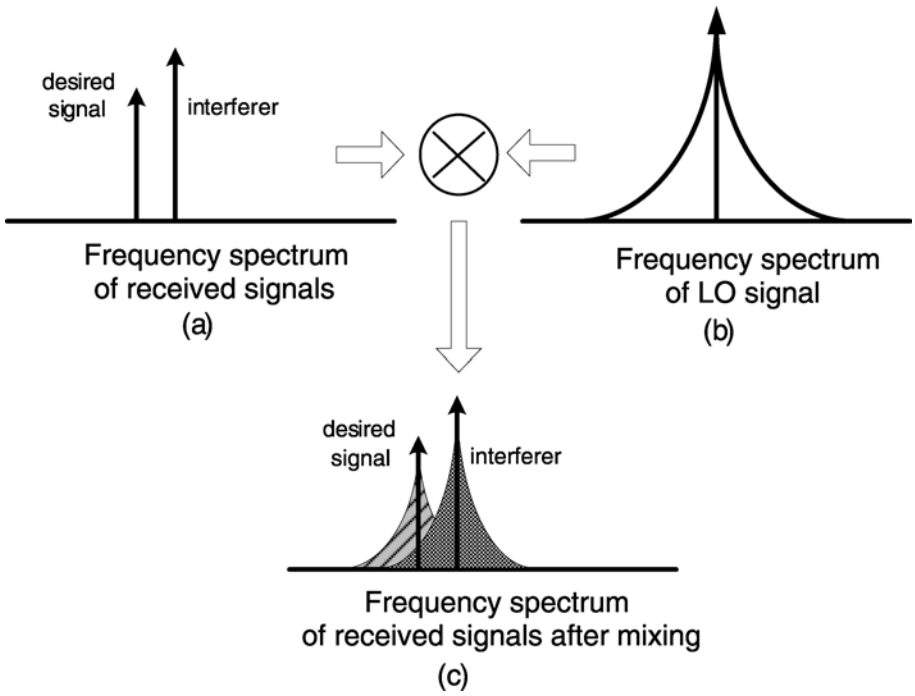

Fig. 2.3 Frequency spectrum of (a) received signal, (b) LO signal with phase noise, and (c) received signal suffering from SNR degradation after mixing

transitions of the oscillator will be accumulated over time, and the oscillator itself cannot recover the phase error. Therefore, the design specification of phase noise for an oscillator is stringent, especially in CMOS technology.

An oscillator's phase error can be shown to increase with measured time when the oscillator is free running. This also leads to a frequency shift. Hence, a control mechanism is required to lock the system and keep it stable (as will be mentioned in detail in Section 2.4).

In fact, phase noise and jitter are related to each other. However, phase noise represented in the frequency domain can give a more detailed picture of how noise contributes at different frequency offsets from the carrier frequency.

Phase noise has been shown to have a Lorentzian spectrum and is depicted as (Poore, 2001)

$$L(\Delta f) \propto \frac{f_o^2}{\left(\alpha \pi f_o^2\right)^2 + \Delta f^2}, \tag{2.4}$$

where f_o is the oscillating frequency and Δf is the frequency offset from the carrier. The noise spectrum falls at -20 dB per decade. However, it does not include flicker noise (or $1/f$ noise) and white noise. Leeson's equation shown in Equation (2.5)

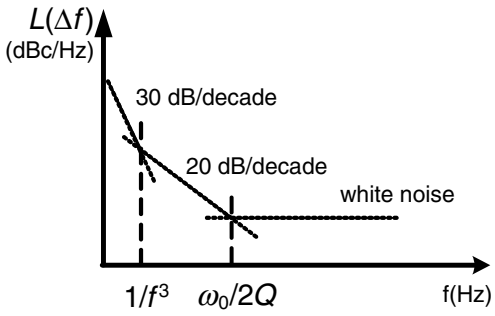

Fig. 2.4 Noise spectrum of typical oscillators

describes the detail of the phase noise spectrum in practical oscillators (Leeson, 1966; Lee, 2000):

$$L(\Delta f) = 10 \log \left[\frac{2FKT}{P_0} \left(1 + \frac{f_0^2}{4Q^2 \Delta f^2} \right) \left(1 + \frac{\Delta f_{1/f^3}}{\Delta f} \right) \right], \tag{2.5}$$

where:

F	is the excess noise factor;
K	is the Boltzmann constant with a value of 1.38×10^{-23} J/K;
T	is the absolute temperature;
P_0	is the power of the carrier signal;
f_0	is the carrier frequency;
Q	is the quality factor in the LC tank;
Δf	is the offset frequency from the carrier frequency;
$\Delta f_{1/f^3}$	is the corner frequency of $1/f$ noise.

Thus, Leeson's model includes flicker noise and the white noise floor. The noise spectrum is depicted in Fig. 2.4.

Lesson's model indicates that typical phase noise falls at -30 dB per decade before the $1/f^3$ frequency corner. This phenomenon occurs because $1/f$ noise modulates the transconductance of the transistors in the oscillator. Compared with bipolar transistor, CMOS devices exhibit a wider $1/f^3$ frequency region because of their higher $1/f$ frequency corners (Razavi, 1996b). Beyond the $1/f^3$ frequency region, the phase noise drops to -20 dB per decade and finally levels off as white noise becomes dominant. The noise floor is mainly contributed by the thermal noise of the devices and results in the phase noise being equal to $2FKT/P_0$.

In the time domain, the oscillating signal $V_{vco}(t)$ with timing jitter can be expressed as

$$V_{vco}(t) = V_o \cos[\omega_o t + \phi(t)], \tag{2.6}$$

where $\phi(t)$ is the phase noise of the oscillator, and V_o is the signal amplitude.

The output can be simplified to

$$V_{vco}(t) = V_o \cos(\omega_o t) - V_o \sin(\omega_o t) \cdot \phi(t). \tag{2.7}$$

If $\phi(t)$ is assumed to be $\phi_A \sin(\omega_\phi t)$, where ϕ_A is the noise amplitude at frequency ω_ϕ, Equation (2.7) can then be expressed as

$$V_{vco}(t) = V_o \cos(\omega_o t) - \frac{V_o \phi_A}{2}[\cos(\omega_o t - \omega_\phi t) - \cos(\omega_o t + \omega_\phi t)]. \tag{2.8}$$

It shows that any noise at low frequency or high frequency can be modulated and appear as the sideband of the carrier in the frequency domain. Thus, noise consideration in oscillator designs should not be limited only to frequencies around the fundamental oscillation frequency.

To design receivers with a required SNR, the phase noise of the oscillator should satisfy the condition

$$L(\Delta\omega) < S_{RF} - S_{block} - 10\log_{10}(\text{BW}) - \text{SNR} \tag{2.9}$$

where:

S_{RF}	is the desired RF signal power;
S_{block}	is the blocking signal power;
BW	is the channel bandwidth of the desired RF signal;
SNR	is the signal-to-noise ratio for a system to achieve the required bit-error rate.

From the system point of view, the maximum power of the blocking signals and thus the phase noise requirement are different at different frequency offsets from the carrier. As a result, the phase noise requirement should be based on the worst case consideration.

2.4. Phase-locked loop

As mentioned in Section 2.2, an oscillator by itself cannot recover the phase error and the frequency shift. However, as long as the phase of the oscillator can be controlled and locked, the frequency can also be locked. This is because the change of the phase with respect to time is equivalent to its frequency. Consequently, a phase-locked loop (PLL) is typically used to lock both the phase and the frequency of the oscillator to provide a stable output signal.

A PLL is a negative feedback system, and a general block diagram of such a system is shown in Fig. 2.5. Basically, a PLL system consists of an input phase detector (PD), a charge pump, a loop filter, a voltage-controlled oscillator (VCO), and dividers. Dividers N and M are optional but may be required depending on the desired ratio between the PLL's output frequency and the reference clock frequency.