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978-0-521-83294-6 - Fundamentals of Modern VLSI Devices: Second Edition
Yuan Taur and Tak H. Ning
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Fundamentals of Modern VLSI Devices

Learn the basic properties and designs of modern VLSI devices, as well as the factors affecting performance, with this thoroughly updated second edition. The first edition has been widely adopted as a standard textbook in microelectronics in many major US universities and worldwide. The internationally renowned authors highlight the intricate interdependencies and subtle tradeoffs between various practically important device parameters. An in-depth discussion of device scaling and scaling limits of CMOS and bipolar devices is also provided. Equations and parameters provided are checked continuously against the reality of silicon data, making the book equally useful in practical transistor design and in the classroom.

New to this edition:

- **Every chapter has been updated** to include the latest developments, such as MOSFET scale length theory, high-field transport models, and SiGe-base bipolar devices.
- **Two new chapters** cover read and write operations of commonly used SRAM, DRAM, and non-volatile memory arrays, as well as silicon-on-insulator (SOI) devices, including advanced devices of future potential.
- **More useful appendices**: The number has doubled from 9 to 18, covering areas such as spatial variation of quasi-Fermi potentials, image-force-induced barrier lowering, and power gain of a two-port network.
- **New homework exercises** at the end of every chapter engage students with real-world problems and test their understanding.

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Fundamentals of Modern VLSI Devices

SECOND EDITION

YUAN TAUR
University of California, San Diego

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Preface to the first edition

It has been fifty years since the invention of the bipolar transistor, more than forty years since the invention of the integrated-circuit (IC) technology, and more than thirty-five years since the invention of the MOSFET. During this time, there has been a tremendous and steady progress in the development of the IC technology with a rapid expansion of the IC industry. One distinct characteristic in the evolution of the IC technology is that the physical feature sizes of the transistors are reduced continually over time as the lithography technologies used to define these features become available. For almost thirty years now, the minimum lithography feature size used in IC manufacturing has been reduced at a rate of 0.7× every three years. In 1997, the leading-edge IC products have a minimum feature size of 0.25 μm.

The basic operating principles of large and small transistors are the same. However, the relative importance of the various device parameters and performance factors for transistors of the 1- μm and smaller generations is quite different from those for transistors of larger-dimension generations. For example, in the case of CMOS, the power-supply voltage was lowered from the standard 5 V, starting with the 0.6- to 0.8- μm generation. Since then CMOS power supply voltage has been lowered in steps once every few years as the device physical dimensions are reduced. At the same time, many physical phenomena, such as short-channel effect and velocity saturation, which are negligible in large-dimension MOSFETs, are becoming more and more important in determining the behavior of MOSFETs of deep-submicron dimensions. In the case of bipolar devices, breakdown voltage and base-widening effects are limiting their performance, and power dissipation is limiting their level of integration on a chip. Also, the advent of SiGe-base bipolar technology has extended the frequency capability of small-dimension bipolar transistors into the range previously reserved for GaAs and other compound-semiconductor devices.

The purpose of this book is to bring together the device fundamentals that govern the behavior of CMOS and bipolar transistors into a single text, with emphasis on those parameters and performance factors that are particularly important for VLSI (very-large-scale-integration) devices of deep-submicron dimensions. The book starts with a comprehensive review of the properties of the silicon material, and the basic physics of p–n junctions and MOS capacitors, as they relate to the fundamental principles of MOSFET and bipolar transistors. From there, the basic operation of MOSFET and bipolar devices, and their design and optimization for VLSI applications are developed. A great deal of the volume is devoted to in-depth discussions of the intricate interdependence and subtle tradeoffs of the various device parameters pertaining to circuit performance and manufacturability. The effects which are particularly important in small-dimension devices,

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e.g., quantization of the two-dimensional surface inversion layer in a MOSFET device and the heavy-doping effect in the intrinsic base of a bipolar transistor, are covered in detail. Also included in this book are extensive discussions on scaling and limitations to scaling of MOSFET and bipolar devices.

This book is suitable for use as a textbook by senior undergraduate or graduate students in electrical engineering and microelectronics. The necessary background assumed is an introductory understanding of solid-state physics and semiconductor physics. For practicing engineers and scientists actively involved in research and development in the IC industry, this book serves as a reference in providing a body of knowledge in modern VLSI devices for them to stay up to date in this field.

VLSI devices are too huge a subject area to cover thoroughly in one book. We have chosen to cover only the fundamentals necessary for discussing the design and optimization of the state-of-the-art CMOS and bipolar devices in the sub-0.5-μm regime. Even then, the specific topics covered in this book are based on our own experience of what the most important device parameters and performance factors are in modern VLSI devices.

Many people have contributed directly and indirectly to the topics covered in this book. We have benefited enormously from the years of collaboration and interaction we had with our colleagues at IBM, particularly in the areas of advanced silicon-device research and development. These include Douglas Buchanan, Hu Chao, T. C. Chen, Wei Chen, Kent Chuang, Peter Cook, Emmanuel Crabbé, John Cressler, Bijan Davari, Robert Dennard, Max Fischetti, David Frank, Charles Hsu, Genda Hu, Randall Isaac, Khalid Ismail, G. P. Li, Shih-Hsien Lo, Yuh-Jier Mii, Edward Nowak, George Sai-Halasz, Stanley Schuster, Paul Solomon, Hans Stork, Jack Sun, Denny Tang, Lewis Terman, Clement Wann, James Warnock, Siegfried Wiedmann, Philip Wong, Matthew Wordeman, Ben Wu, and Hwa Yu.

We would like to acknowledge the secretarial support of Barbara Grady and the support of our management at IBM Thomas J. Watson Research Center where this book was written. Finally, we would like to give special thanks to our families – Teresa, Adrienne, and Brenda Ning and Betty, Ying, and Hsuan Taur – for their support and understanding during this seemingly endless task.

Yuan Taur
Tak H. Ning
Yorktown Heights, New York, October, 1997

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Preface to the second edition

Since the publication of the first edition of *Fundamentals of Modern VLSI Devices* by Cambridge University Press in 1998, we received much praise and many encouraging reviews on the book. It has been adopted as a textbook for first-year graduate courses on microelectronics in many major universities in the United States and worldwide. The first edition was translated into Japanese by a team led by Professor Shibahara of Hiroshima University in 2002.

During the past 10 years, the evolution and scaling of VLSI (very-large-scale-integration) technology has continued. Now, sixty years after the first invention of the transistor, the number of transistors per chip for both microprocessors and DRAM (dynamic random access memory) has increased to over one billion, and the highest clock frequency of microprocessors has reached 5 GHz. In 2007, the worldwide IC (integrated circuits) sales grew to $250 billion. In 2008, the IC industry reached the 45-nm generation, meaning that the leading-edge IC products employ a minimum lithography feature size of 45 nm. As bulk CMOS (complementary metal–oxide–semiconductor field-effect transistor) technologies are scaled to dimensions below 100 nm, the very factor that makes CMOS technology the technology of choice for digital VLSI circuits, namely, its low standby power, can no longer be taken for granted. Not only has the off-state current gone up with the power supply voltage down scaled to the 1 V level, the gate leakage has also increased exponentially from quantum mechanical tunneling through gate oxides only a few atomic layers thick. Power management, both active and standby, has become a key challenge to continued increase of clock frequency and transistor count in microprocessors. New materials and device structures are being explored to replace conventional bulk CMOS in order to extend scaling to 10 nm.

The purpose of writing the second edition is to update the book with additional material developed after the completion of the first edition. Key new material added includes MOSFET scale length theory and high-field transport model, and the section on SiGe-base bipolar devices has been greatly expanded. We have also expanded the discussions on basic device physics and circuits to include metal–silicon contacts, noise margin of CMOS circuits, and figures of merit for RF applications. Furthermore, two new chapters are added to the second edition. Chapter 9 is on memory devices and covers the fundamentals of read and write operations of commonly used SRAM, DRAM, and nonvolatile memory arrays. Chapter 10 is on silicon-on-insulator (SOI) devices, including advanced devices of future potential.

We would like to take this opportunity to thank all the friends and colleagues who gave us encouragement and valuable suggestions for improvement of the book. In particular, Professor Mark Lundstrom of Purdue University who adopted the first edition early on,

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and Dr. Constantin Bulucea of National Semiconductor Corporation who suggested the treatment on diffusion capacitance. Thanks also go to Professor James Meindl of Georgia Institute of Technology, Professor Peter Asbeck of University of California, San Diego, and Professor Jerry Fossum of University of Florida for their support of the book.

We would like to thank many of our colleagues at IBM, particularly in the areas of advanced silicon-device research and development, for their direct or indirect contributions. Yuan Taur would like to thank many of his students at University of California, San Diego, in particular Jooyoung Song and Bo Yu, for their help with the completion of the second edition. He would also like to thank Katie Kahng for her love, support, and patience during the course of the work.

We would like to give special thanks to our families for their support and understanding during this seemingly endless task.

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Physical constants and unit conversions

Description	Symbol	Value and unit
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	1.38×10^{-23} J/K
Vacuum permittivity	ε_0	8.85×10^{-14} F/cm
Silicon permittivity	ε_{si}	1.04×10^{-12} F/cm
Oxide permittivity	ε_{ox}	3.45×10^{-13} F/cm
Velocity of light in vacuum	c	3×10^{10} cm/s
Planck's constant	h	6.63×10^{-34} J-s
Free-electron mass	m_0	9.1×10^{-31} kg
Thermal voltage ($T = 300$ K)	kT/q	0.0259 V
Angstrom	Å	1Å = 10^{-8} cm
Nanometer	nm	1 nm = 10^{-7} cm
Micrometer (micron)	μm	1 μm = 10^{-4} cm
Millimeter	mm	1 mm = 0.1 cm
Meter	m	1 m = 10^2 cm
Electron-volt	eV	1eV = 1.6×10^{-19} J
Energy = charge × voltage	$E = qV$	Joule = Coulomb × Volt
Charge = capacitance × voltage	$Q = CV$	Coulomb = Farad × Volt
Power = current × voltage	$P = IV$	Watt = Ampere × Volt
Time = resistance × capacitance	$t = RC$	second = Ω (ohm) × Farad
Current = charge/time	$I = Q/t$	Ampere = Coulomb/second
Resistance = voltage/current	$R = V/I$	Ω (ohm) = Volt/Ampere

A word of caution about the length units: strictly speaking, MKS units should be used for all the equations in the book. As a matter of convention, electronics engineers often work with centimeter as the unit of length. While some equations work with lengths in either meter or centimeter, not all of them do. It is prudent always to check for unit consistency when doing calculations. It may be necessary to convert the length unit to meter before plugging into the equations.

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List of symbols

Symbol	Description	Unit
A	Area	cm^2
A_E	Emitter area	cm^2
α	Common-base current gain	None
α_0	Static common-base current gain	None
α_F	Forward common-base current gain in the Ebers–Moll model	None
α_R	Reverse common-base current gain in the Ebers–Moll model	None
α_T	Base transport factor	None
α_n	Electron-initiated rate of electron–hole pair generation per unit distance	cm^{-1}
α_p	Hole-initiated rate of electron–hole pair generation per unit distance	cm^{-1}
BV	Breakdown voltage	V
BV_{CBO}	Collector–base junction breakdown voltage with emitter open circuit	V
BV_{CEO}	Collector–emitter breakdown voltage with base open circuit	V
BV_{EBO}	Emitter–base junction breakdown voltage with collector open circuit	V
β	Current gain	None
β_0	Static common-emitter current gain	None
β_F	Forward common-emitter current gain in the Ebers–Moll model	None
β_R	Reverse common-emitter current gain in the Ebers–Moll model	None
c	Velocity of light in vacuum ($= 3 \times 10^{10}$ cm/s)	cm/s
C	Capacitance	F
C_d	Depletion-layer capacitance per unit area	F/cm^2
$C_{d,tot}$	Total depletion-layer capacitance	F
C_{dBC}	Base–collector diode depletion-layer capacitance per unit area	F/cm^2
$C_{dBC,tot}$	Total base–collector diode depletion-layer capacitance	F
C_{dBE}	Base–emitter diode depletion-layer capacitance per unit area	F/cm^2
$C_{dBE,tot}$	Total base–emitter diode depletion-layer capacitance	F
C_{dm}	Maximum depletion-layer capacitance (per unit area)	F (F/cm^2)
C_D	Diffusion capacitance	F

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C_{Dn}	Diffusion capacitance due to excess electrons	F
C_{Dp}	Diffusion capacitance due to excess holes	F
C_{DE}	Emitter diffusion capacitance	F
C_{DoS}	Equivalent density-of-states capacitance	F/m^2
C_{fb}	MOS capacitance at flat band per unit area	F/cm^2
C_{FC}	Capacitance between the floating gate and the control gate of a MOSFET nonvolatile memory device	F
C_g	Intrinsic gate capacitance per unit area	F/cm^2
C_G	Total gate capacitance of MOSFET	F
C_i	Inversion-layer capacitance per unit area	F/cm^2
C_{it}	Interface trap capacitance per unit area	F/cm^2
C_j	Junction capacitance per unit area	F/cm^2
C_J	Junction capacitance	F
C_L	Load capacitance	F
C_{in}	Equivalent input capacitance of a logic gate	F
C_{inv}	MOSFET capacitance in inversion per unit area	F/cm^2
$C_{\min}$	Minimum MOS capacitance per unit area	F/cm^2
C_{out}	Equivalent output capacitance of a logic gate	F
C_{ov}	Gate-to-source (-drain) overlap capacitance (per edge)	F
C_{ox}	Oxide capacitance per unit area	F/cm^2
C_p	Polysilicon-gate depletion-layer capacitance per unit area	F/cm^2
C_{si}	Silicon capacitance per unit area	F/cm^2
C_w	Wire capacitance per unit length	F/cm
C_π	Base–emitter capacitance in the small-signal hybrid-π equivalent-circuit model	F
C_μ	Base–collector capacitance in the small-signal hybrid-π equivalent-circuit model	F
d	Width of diffusion region in a MOSFET	cm
D_n	Electron diffusion coefficient	cm^2/s
D_{nB}	Electron diffusion coefficient in the base of an n–p–n transistor	cm^2/s
D_p	Hole diffusion coefficient	cm^2/s
D_{pE}	Hole diffusion coefficient in the emitter of an n–p–n transistor	cm^2/s
ΔV_t	Threshold voltage rolloff due to short-channel effect	V
ΔE_g	Apparent bandgap narrowing	J
ΔE_{gB}	Bandgap-narrowing parameter in the base region	J
$\Delta E_{g,\max}$	Maximum bandgap narrowing due to the presence of Ge	J
$\Delta E_{g,SiGe}$	Local bandgap narrowing due to the presence of Ge	J
ΔL	Channel length modulation in MOSFET	cm
ΔQ_{total}	Total charge stored in a nonvolatile memory device	C
E	Energy	J
E_c	Conduction-band edge	J
E_v	Valence-band edge	J
E_a	Ionized-acceptor energy level	J

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E_d	Ionized-donor energy level	J
E_f	Fermi energy level	J
E_g	Energy gap of silicon	J
E_i	Intrinsic Fermi level	J
E_{fn}	Fermi energy level on the n-side of a p–n diode	J
E_{fp}	Fermi energy level on the p-side of a p–n diode	J
$\mathscr{E}$	Electric field	V/cm
$\mathscr{E}_c$	Critical field for velocity saturation	V/cm
$\mathscr{E}_{eff}$	Effective vertical field in MOSFET	V/cm
$\mathscr{E}_{ox}$	Oxide electric field	V/cm
$\mathscr{E}_s$	Electric field at silicon surface	V/cm
$\mathscr{E}_x$	Vertical field in silicon	V/cm
$\mathscr{E}_y$	Lateral field in silicon	V/cm
ε_0	Vacuum permittivity ($= 8.85 \times 10^{-14}$ F/cm)	F/cm
ε_i	Permittivity of gate insulator	F/cm
ε_{si}	Silicon permittivity ($= 1.04 \times 10^{-12}$ F/cm)	F/cm
ε_{ox}	Oxide permittivity ($= 3.45 \times 10^{-13}$ F/cm)	F/cm
f_D	Probability that an electronic state is filled	None
f	Frequency, clock frequency	Hz
$f_{\max}$	Unity power gain frequency	Hz
f_T	Unity current gain frequency	Hz
FI	Fan-in	None
FO	Fan-out	None
ϕ	Barrier height	V
ϕ_{ox}	Silicon–silicon dioxide interface potential barrier for electrons	V
ϕ_{ms}	Work-function difference between metal and silicon	V
ϕ_n	Electron quasi-Fermi potential	V
ϕ_p	Hole quasi-Fermi potential	V
ϕ_{Bn}	Schottky barrier height for electrons	V
ϕ_{Bp}	Schottky barrier height for holes	V
g	Number of degeneracy	None
g_{ds}	Small-signal output conductance	A/V
g_m	Small-signal transconductance	A/V
G_E	Emitter Gummel number	s/cm^4
G_B	Base Gummel number	s/cm^4
G_n	Electron emission rate (also called electron generation rate)	1/cm^3-s
G_p	Hole emission rate (also called hole generation rate)	1/cm^3-s
γ	Emitter injection efficiency	None
h	Planck's constant ($= 6.63 \times 10^{-34}$ J-s)	J-s
i	Time-dependent current	A
i_B	Time-dependent base current in a bipolar transistor	A
i_b	Time-dependent small-signal base current	A
i_C	Time-dependent collector current in a bipolar transistor	A

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i_c	Time-dependent small-signal collector current	A
i_E	Time-dependent emitter current in a bipolar transistor	A
I	Current	A
I_B	Static base current in a bipolar transistor	A
I_C	Static collector current in a bipolar transistor	A
I_E	Static emitter current in a bipolar transistor	A
I_S	Switch current in an ECL circuit	A
I_g	Gate current in a MOSFET	A
I_0	MOSFET current per unit width to length ratio for threshold definition	A
I_{dsat}	MOSFET saturation current	A
I_{on}	MOSFET on current	A
I_{off}	MOSFET off current	A
I_n	nMOSFET current per unit width	A/cm
I_p	pMOSFET current per unit width	A/cm
I_N	nMOSFET current	A
I_P	pMOSFET current	A
I_{ds}	Drain-to-source current in a MOSFET	A
I_{sx}	Substrate current in a MOSFET	A
$I_{ds,Vt}$	MOSFET current at threshold	A
$I_{on,n}$	nMOSFET on current per device width	A/cm
I_{onN}	nMOSFET on current	A
$I_{on,p}$	pMOSFET on current per device width	A/cm
I_{onP}	pMOSFET on current	A
λ	MOSFET scale length	cm
J	Current density	A/cm^2
J_B	Base current density	A/cm^2
J_C	Collector current density	A/cm^2
J_n	Electron current density	A/cm^2
J_p	Hole current density	A/cm^2
k	Boltzmann's constant ($= 1.38 \times 10^{-23}$ J/K)	J/K
κ	Scaling factor (> 1)	None
l	Mean free path	cm
L	Length, MOSFET channel length	cm
L_D	Debye length	cm
L_n	Electron diffusion length	cm
L_p	Hole diffusion length	cm
L_{met}	Metallurgical channel length of MOSFET	cm
L_{eff}	Effective channel length of MOSFET	cm
L_w	Wire length	cm
m	MOSFET body-effect coefficient	None
m_0	Free-electron mass ($= 9.1 \times 10^{-31}$ kg)	kg
m^*	Electron effective mass	kg

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M	Avalanche multiplication factor	None
m_l	Electron effective mass in the longitudinal direction	kg
m_t	Electron effective mass in the transverse direction	kg
μ	Carrier mobility	$cm^2/V\text{-}s$
μ_{eff}	Effective mobility	$cm^2/V\text{-}s$
μ_n	Electron mobility	$cm^2/V\text{-}s$
μ_p	Hole mobility	$cm^2/V\text{-}s$
n	Density of free electrons	cm^{-3}
n_0	Density of free electrons at thermal equilibrium	cm^{-3}
n_i	Intrinsic carrier density	cm^{-3}
n_{ie}	Effective intrinsic carrier density	cm^{-3}
n_{ieB}	Effective intrinsic carrier density in base of bipolar transistor	cm^{-3}
n_{ieE}	Effective intrinsic carrier density in emitter of bipolar transistor	cm^{-3}
n_n	Density of electrons in n-region	cm^{-3}
n_p	Density of electrons in p-region	cm^{-3}
N_a	Acceptor impurity density	cm^{-3}
N_d	Donor impurity density	cm^{-3}
N_b	Impurity concentration in bulk silicon	cm^{-3}
N_c	Effective density of states of conduction band	cm^{-3}
N_v	Effective density of states of valence band	cm^{-3}
N_B	Base doping concentration	cm^{-3}
N_C	Collector doping concentration	cm^{-3}
N_E	Emitter doping concentration	cm^{-3}
$N(E)$	Density of electronic states per unit energy per volume	$1/J\text{-}m^3$
p	Density of free holes	cm^{-3}
p_0	Density of free holes at thermal equilibrium	cm^{-3}
p_n	Density of holes in n-region	cm^{-3}
p_p	Density of holes in p-region	cm^{-3}
P	Power dissipation	W
P_{ac}	Active power dissipation	W
P_{off}	Standby power dissipation	W
q	Electronic charge ($= 1.6 \times 10^{-19}$ C)	C
Q	Charge	C
Q_B	Excess minority charge per unit area in the base	C/cm^2
$Q_{B,tot}$	Total excess minority charge in the base	C
Q_{BE}	Excess minority charge per unit area in the base–emitter space-charge region	C/cm^2
$Q_{BE,tot}$	Total excess minority charge in the base–emitter space-charge region	C
Q_{BC}	Excess minority charge per unit area in the base–collector space-charge region	C/cm^2
$Q_{BC,tot}$	Total excess minority charge in the base–collector space-charge region	C

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Q_{DE}	Total stored minority-carrier charge in a bipolar transistor biased in the forward-active mode	C
Q_E	Excess minority charge per unit area in the emitter	C/cm^2
$Q_{E,tot}$	Total excess minority charge in the emitter	C
Q_{pB}	Hole charge per unit area in base of n–p–n transistor	C/cm^2
Q_s	Total charge per unit area in silicon	C/cm^2
Q_d	Depletion charge per unit area	C/cm^2
Q_i	Inversion charge per unit area	C/cm^2
Q_f	Fixed oxide charge per unit area	C/cm^2
Q_g	Charge on MOS gate per unit area	C/cm^2
Q_m	Mobile charge per unit area	C/cm^2
Q_{it}	Interface trapped charge per unit area	C/cm^2
Q_n	Excess electron charge per unit area	C/cm^2
Q_{ot}	Oxide trapped charge per unit area	C/cm^2
Q_{ox}	Equivalent oxide charge density per unit area	C/cm^2
Q_p	Excess hole charge per unit area	C/cm^2
r, R	Resistance	Ω
r_b	Base resistance	Ω
r_{bi}	Intrinsic base resistance	Ω
r_{bx}	Extrinsic base resistance	Ω
r_c	Collector series resistance	Ω
r_e	Emitter series resistance	Ω
r_0	Output resistance in small-signal hybrid-π equivalent-circuit model	Ω
r_π	Input resistance in small-signal hybrid-π equivalent-circuit model	Ω
R_L	Load resistance in a circuit	Ω
R_s	Source series resistance	Ω
R_d	Drain series resistance	Ω
R_n	Electron capture rate (also called electron recombination rate)	1/cm^3-s
R_p	Hole capture rate (also called hole recombination rate)	1/cm^3-s
R_{sd}	Source–drain series resistance	Ω
R_{ch}	MOSFET channel resistance	Ω
R_w	Wire resistance per unit length	Ω/cm
R_{Sbi}	Sheet resistance of intrinsic-base layer	Ω/□
R_{sw}	Equivalent switching resistance of a CMOS gate	Ω
R_{swn}	Equivalent switching resistance of nMOSFET pulldown	Ω
R_{swp}	Equivalent switching resistance of pMOSFET pullup	Ω
ρ	Resistivity	Ω-cm
ρ_{sh}	Sheet resistivity	Ω/□
ρ_{ch}	Sheet resistivity of MOSFET channel	Ω/□
ρ_{sd}	Sheet resistivity of source or drain region	Ω/□
ρ_c	Specific contact resistivity	Ω-cm^2

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ρ_{net}	Volume density of net charge	C/cm^3
S	MOSFET inverse subthreshold current slope	V/decade
S_p	Surface recombination velocity for holes	cm/s
σ_L	Lateral straggle of Gaussian doping profile	cm
t	Time	s
t_B	Base transit time	s
t_E	Emitter transit time	s
t_{BE}	Base–emitter depletion-layer transit time	s
t_{BC}	Base–collector depletion-layer transit time	s
t_i	Thickness of gate insulator	cm
t_{inv}	Equivalent oxide thickness for inversion charge calculations	cm
t_{ox}	Oxide thickness	cm
t_r	Transit time	s
t_w	Thickness of wire	cm
t_{si}	Thickness of silicon film	cm
T	Absolute temperature	K
τ	Lifetime	s
τ	Circuit delay	s
τ_b	Buffered delay	s
τ_{int}	Intrinsic, unloaded delay	s
τ_F	Forward transit time of bipolar transistor	s
τ_n	Electron lifetime	s
τ_n	nMOSFET pulldown delay	s
τ_{nB}	Electron lifetime in base of n–p–n transistor	s
τ_p	Hole lifetime	s
τ_p	pMOSFET pullup delay	s
τ_{pE}	Hole lifetime in emitter of n–p–n transistor	s
τ_R	Reverse transit time of bipolar transistor	s
τ_w	Wire *RC* delay	s
τ_E	Emitter delay time	s
τ_B	Base delay time	s
τ_{BE}	Base–emitter depletion-region delay time	s
τ_{BC}	Base–collector depletion-region delay time	s
U	Net recombination rate	1/cm^3-s
v	Velocity	cm/s
v	Small-signal voltage	V
v_{th}	Thermal velocity	cm/s
v_d	Carrier drift velocity	cm/s
v_{sat}	Saturation velocity of carriers	cm/s
v_T	Thermal injection velocity at MOSFET source	cm/s
V	Voltage	V
V	Quasi-Fermi potential along MOSFET channel	V
V_A	Early voltage	V

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V_{app}	Applied voltage across p–n diode	V
V'_{app}	Applied voltage appearing immediately across p–n junction (smaller than V_{app} by IR drops in series resistances)	V
V_{BE}	Base–emitter bias voltage	V
V_{BC}	Base–collector bias voltage	V
V_{CE}	Collector-to-emitter voltage	V
V_{CG}	Control gate voltage in a nonvolatile memory device	V
V_{FG}	Floating gate voltage in a nonvolatile memory device	V
V_{dd}	Power-supply voltage	V
V_{ds}	Source-to-drain voltage	V
V_{dsat}	MOSFET drain saturation voltage	V
V_{fb}	Flat-band voltage	V
V_{ox}	Potential drop across oxide	V
V_g	Gate voltage in MOS	V
V_{gs}	Gate-to-source voltage in a MOSFET	V
V_{bs}	MOSFET body bias voltage	V
V_t	Threshold voltage ($2\psi_B$ definition)	V
V_{on}	Linearly extrapolated threshold voltage	V
V_{in}	Input node voltage of a logic gate	V
V_{out}	Output node voltage of a logic gate	V
V_x	Node voltage between stacked nMOSFETs of a NAND gate	V
$V_{t,high}$	The higher threshold voltage of a nonvolatile memory device	V
$V_{t,low}$	The lower threshold voltage of a nonvolatile memory device	V
W	Width, MOSFET width	cm
W_n	nMOSFET width	cm
W_p	pMOSFET width	cm
W_B	Intrinsic-base width	cm
W_d	Depletion-layer width	cm
W_{dBE}	Base–emitter junction depletion-layer width	cm
W_{dBC}	Base–collector junction depletion-layer width	cm
W_{dm}	Maximum depletion-layer width in MOS	cm
W_E	Emitter-layer width (thickness)	cm
W_S	Source junction depletion-layer width	cm
W_D	Drain junction depletion-layer width	cm
ω	Angular frequency	rad/s
x_j	Junction depth	cm
x_c, x_i	Depth of inversion channel	cm
ψ	Potential	V
ψ_B	Difference between Fermi potential and intrinsic potential	V
ψ_{bi}	Built-in potential	V
ψ_f	Fermi potential	V
ψ_i	Intrinsic potential	V
ψ_s	Surface potential	V

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