1

Semiconducting materials

1.1 Materials development and crystal growth techniques

This chapter outlines the nature and importance of semiconductors. The industrially important semiconductors are tetrahedrally coordinated, diamond and related structure IVB, III-V and related materials. The sp^3 tetrahedral covalent bonding is stiff and brittle, unlike the metallic bond, which merely requires closest packing to minimize the energy. The atomic core structures of extended defects in semiconductors depend on this stiff, brittle bonding and in turn give rise to the electrical and optical properties of defects.

The semiconductors' closely related adamantine (diamond-like) crystal structures and energy band diagrams are outlined. There are a large number of families of such semiconducting compounds and alloys, some of which are non-crystalline. However, only a few have been developed to the highest levels of purity and perfection so that single crystal wafers are available. Instead, with modern epitaxial growth techniques, thin films, quantum wells, wires and dots and artificial superlattices can be produced. This can be done with many semiconductor materials, including alloys of continuously variable composition, with the necessary quality on one of the few available types of wafer. These epitaxial materials have 'engineered' energy band structures and hence electronic and optoelectronic properties and can be designed for incorporation into devices to meet new needs. It is largely to this field that materials development has moved, except for the occasional development of an additional material like GaN.

The chapter closes with a brief account of the way that competitive materials development, responding to economic demand, determines which materials enter production. Cases of materials competition covered include those of Si vs. Ge, of III-Vs vs. Si, and of GaN versus other electroluminescent III-V compounds and alloys.

Semiconductors (half conductors) originally meant materials with conductivities between those typical of metals and of insulators. However, this definition would,

Table 1.1. *Typical conductivity (at room-temperature) ranges attainable by doping particular cyberconductors*

	Conductivity $(\Omega\text{-cm})^{-1}$	
Material	Heavily doped n^+ and p^+	Intrinsic or compensated
Si	$\sim 10^{+3}$ n and p	$\sim 10^{-4}$
Ge	$\sim 2 \times 10^{+3}$ n and p	$\sim 2 \times 10^{-2}$
GaAs	$\sim 10^{+3}$ p and 10^{+4} n type	$\sim 10^{-8}$ (semi-insulating)

strictly, include both electronic and 'fast ionic' (superionic) conductors. Moreover, the conductivity of any semiconductor can be varied in sign and magnitude over a wide range (see Table 1.1). They have high resistivities at room temperature when pure (intrinsic) but can be given large conductivities by impurity doping them *n*- or *p*-type. This makes the production of microelectronic devices and integrated circuits possible. Also the conductivity can be controlled during device operation by injecting additional carriers through a contact such as that to the base of a bipolar transistor or by shining light on a photoconductive or photovoltaic detector. Thus the essential feature of semiconductors is not that they are 'semi' (half) conductors but that they are 'cyber' (controllable, changeable) conductors. (Cyber is from a Greek root word, meaning steersman, and is used in the same way as in 'cybernetics' (the science of feedback and control.)) This behaviour has historically come to be identified with a particular group of materials, including diamond, which, except when doped, is the best insulator known.

1.1.1 Microelectronics and microphotonics

Cyberconductivity is exploited in discrete solid state electronic devices and in microelectronic integrated circuits that are basic to electronics: the technology that manipulates electrons.

There is a second, rapidly growing, field of application of these magical materials: photonics, i.e. the technology that manipulates photons. In this field their important properties are their ability to emit, detect and controllably transmit light, i.e. they are not only 'cyber' conductors but also 'cyber' emitters.

1.1.2 Cyberconductors

Research on germanium led to the invention of transistors and the rise of solid state electronics. Silicon became dominant with the invention of planar technology for integrated circuits. The III-V compounds and alloys dominate in optoelectronics including lightwave communications. This story of materials development and

competition is recounted in Section 1.8. The crystal structures, chemical bonding and electronic energy band structures of these materials are all diamond-like. This book is essentially concerned with the deviations from crystalline perfection in real crystals of these dominant practical cyberconductors, the adamantine materials.

Defects generally strongly affect semiconductor properties and the operation of semiconductor devices. This is because defects in a semiconductor may introduce energy levels (in the forbidden energy gap) affecting the electronic properties of the material. They may also result in device degradation and failure during operation.

The most important application of semiconductors is that for the manufacture of integrated circuits for microelectronics. This uses Si in the form of large crystals of the highest purity and perfection of any material. Semiconductors, however, are not always employed in this form. Devices that must be large in area at a low cost do not employ single crystals of adamantine semiconductors. Examples are found in electrophotographic reproduction (reprographics or xerography including laser printers), lighting and displays, and terrestrial solar photovoltaic power generation. Reprography usually employs layers of non-crystalline ('amorphous') Se or of polycrystalline or powdered ZnO or polymer coatings. Lighting and displays use powder phosphor materials of many kinds in fluorescent lights, CRT and TV screens and electroluminescent display panels. Terrestrial photovoltaic devices employ poly- and non-crystalline Si or compound heterojunctions, as will be discussed in Section 1.7.5 and Section 1.8. So defects like grain boundaries and powder particle surfaces can sometimes be tolerated.

Recent developments have drawn attention to the fact that the cyberconductors are also cyberoptical materials. That is, many of these materials are also intermediate between metals (opaque and metallically shiny) and insulators (transparent or translucent). Moreover, they can be made to emit or detect light. Also, while transmitting light, their electrooptical properties can be exploited to process signals in the form of light.

To measure the intrinsic properties of cyberconductors and gain an understanding of semiconductor physics it was first necessary to grow sufficiently pure and perfect crystals. Defect microstructure could then be resolved and its effects on physical properties studied. The impressive improvement of the Czochralski growth technique and the invention of zone refining and methods of controlled doping were other necessary preconditions for both semiconductor science and technology.

Zone refining (Pfann 1952), developed for Ge in the late 1940s, also worked for Si. Narrow molten zones were run along a bar of the material pulled through a furnace with narrow hot zones. The electrically important impurities in Ge and Si fortunately had higher solubilities in the liquid zones than in the solid. Hence they were swept along and accumulated in the end of the rod which was cut off. Much higher purities than ever before were first reached so the properties of intrinsic Ge (and later Si) could be observed. It also made it possible to investigate the effects of controlled doping on these properties. Now, however, the necessary

purification takes place in the gaseous phases occurring in the extraction of these elements from their ores.

Many techniques of *crystal growth* were developed to produce the relatively large and perfect single crystals needed to determine the basic properties of the new semiconductors that were being discovered in the early post-Second World War period (see e.g. the books of Pamplin 1980 and Brice 1986). Such methods produce controlled crystal growth and can be classified according to whether this is from liquid or gaseous material. For semiconductors, the most important methods are the Czochralski (Fig. 1.1) and Bridgman methods of growth from melt, and the liquid, vapour phase and molecular beam methods of epitaxial growth of thin films. Bridgman growth employs a long container or 'boat' drawn through a furnace (horizontally or vertically), so a single crystal grows from a nucleus at the end where freezing starts.

Czochralski growth from melts (named for the Polish worker who originated it) proved best able to be scaled up and it is now the method in industrial use for producing large silicon crystals to be sliced into wafers. Czochralski crystal 'pulling' is shown schematically in Fig. 1.1. Automated Czochralski growth, using feedback

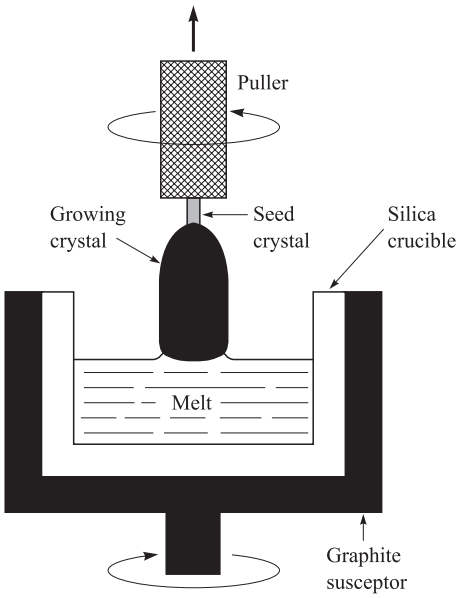

Figure 1.1 Schematic illustration of a Czochralski crystal growth mehtod. A seed crystal gripped by a vertical rod is dipped into the melt and slowly raised while being rotated. Molten material freezes at the seed interface as heat is extracted by conduction up the rod and by radiation outward from the rising crystal. During growth the crucible is raised to maintain the melt surface at a constant height in the furnace. (The growth chamber and the RF inductive heating coils are not shown.)

control to keep the cylindrical 'boules' constant in diameter is used for growing crystals to be sawn and polished into wafers of Si. Annual world production of Czochralski silicon crystals already by the mid 1980s was estimated to be 4000 to 5000 tonnes per annum (e.g. Brice, 1986). The boules are sawn and polished into slices or wafers, totalling about half this mass. This final 1986 total of ~2000 tonnes of Si wafers, each ~500 μm thick thus covered a total area of 1 km^2! Obviously the world output of single crystal silicon for the production of integrated circuits (ICs) and other devices is now much greater than these earlier figures.

Si and Ge can be pulled in vacuum or under inert or reducing atmospheres but at their melting points III-V compounds present dangerously high pressures of their toxic constituent gases. Floating a layer of relatively insoluble boric oxide on the surface of the molten compound was found to be a practical method to reduce this volatility. Crystals pulled through this layer are said to be 'encapsulated' in boric oxide. Most of the slices of III-V compounds available are of such 'liquid encapsulated Czochralski' (LEC) material. The only semiconductors of which large enough crystals to provide slices are available today are Si, Ge, GaAs, GaP, GaSb and InP (and, in the past, InSb). To give an idea of the 'state of the art': at the time of writing the Si IC industry is re-equipping to use 300 mm (12 inch) diameter slices. The most developed III-V compound GaAs is used in industry as 100 or (mainly) 150 mm (6 inch) wafers while 200 mm (8 inch) slices are becoming available. The reason more semiconductors have not been developed to this level is the cost. The late Prof. C. H. L. Goodman used to say that such research and development efforts are so great that the natural unit involved is the man-millenium (thousand man years)!

Recent progress and some of the present issues in materials development and crystal growth techniques were outlined in reviews by Hurle and Rudolph (2004) and Mullin (2004) (see Section 6.5 and Section 6.6). For scaling-up crystal diameter, the former note, among other issues (see Section 6.6), a need for improved furnace design to reduce the dislocation density in the larger crystals. In a review on the melt growth of III-V compounds, Mullin (2004) described the advances, advantages and practical limitations of the liquid encapsulation, vertical gradient freeze, vapour pressure controlled Czochralski and hot wall pulling growth techniques.

The range of materials and properties available to the semiconductor device industry, however, is greatly increased by two things. These are epitaxial growth and the quantum confined structures made possible by it, as we shall now see.

1.1.3 Epitaxy

Prior to the invention of planar technology, integrated circuits and the rise of the silicon solid state electronics industry, epitaxy was of minor academic interest. Si integrated circuits are made by processing carried out only on one face of flat, circular wafers. This planar technology is now universally used for semiconductor

microelectronics and optoelectronics device fabrication. The epitaxial growth of a differently doped Si layer on a Si slice was found to make possible valuable new 'abrupt' *p-n* junctions (i.e. junctions with very rapid, short-range changes from *n*- to *p*-type doping). These could not be obtained by the alternative in-diffusion or ion implantation methods.

The only III-V compound wafers available are of LEC material. These, it was found, cannot be used to make devices due to the presence of unknown and uncontrolled point and other defects. Fortunately, it was found that III-V layers of device quality could be produced by epitaxy. LEC slices are, therefore, used only as substrates on which to grow such epitaxial layers. III-V devices are exclusively fabricated in such material so epitaxy has become a vital semiconductor production technique.

Epitaxy is oriented overgrowth, i.e. the growth of one crystal on another in a single, well-defined, related orientation. (Si on Si growth is thus not, strictly speaking, epitaxy at all. It has been dubbed 'homoepitaxy'.) Using a single crystal substrate and the correct epitaxial growth conditions, therefore, a monocrystalline deposit can be obtained. Two cubic materials, like any pair of the most important semiconductors, usually grow epitaxially with the simple parallel orientation relationship. For general accounts see Matthews (1975), Stradling and Klipstein (1990), Pashley (1991), Davies and Williams (1994), Bachmann (1995), and Mahajan and Sree Harsha (1999).

In addition to the use of epitaxial deposition to produce abrupt Si 'homoepitaxial' *p-n* junctions, and to grow good III-V material on unusable LEC wafers it is also used to produce heterojunctions (interfaces between two different semiconducting materials). The deposited material can be an alloy of two or more III-V compounds, of continuously variable composition. Repeated epitaxial growth of thin layers of different semiconductors is possible. It produces a 'single crystal', i.e. material with a single crystallographic orientation consisting of an epitaxial layered structure. This can be used to produce band gap engineered device structures and quantum confined structures like quantum wells as will be discussed later. This additional vast range of new possibilities removed any continuing necessity to develop new semiconducting compounds to obtain new properties. Consequently, except for GaN, no new compound has been developed in recent decades. Thin films can be deposited epitaxially from the liquid or vapour phase or by molecular beam methods.

Vapour phase epitaxy (VPE) is produced by chemical vapour deposition (CVD); that is by reactions of gases on heated wafers in equipment like that in Fig. 1.2. This has been essentially replaced by a later, superior variant, MOVPE (metal organic VPE, sometimes known as MOCVD, i.e. MO chemical vapour deposition), in which the elements required are provided by the reactions of metal organic precursor gases. For further information see Stringfellow (1989). This can grow more complex III-V alloys and quantum well structures, etc. Doping impurity gases can be added, computer-operated valves can control flow to grow any numbers and thicknesses of

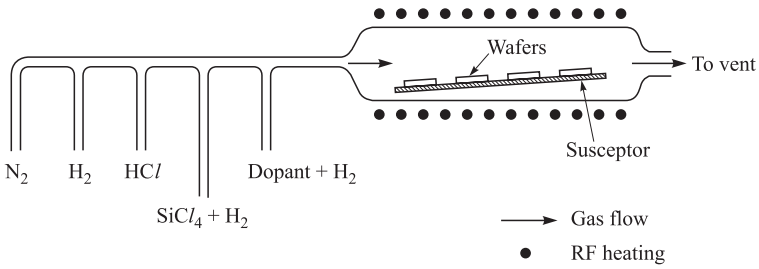

Figure 1.2 Schematic diagram of a reactor for the epitaxial growth of silicon by the hydrogen reduction of silicon tetrachloride. (After Sze 1985; *Semiconductor Devices: Physics and Technology*; Copyright 1985. Reprinted with permission of John Wiley & Sons, Inc.) Other chemical vapour deposition techniques are modified according to the gases involved.

successive thin films. Finally, the thermodynamics of the reactions is understood, so the process can be optimized.

In *liquid phase epitaxy (LPE)* of III-V compounds, substrates held in a carbon 'slider' are pushed under a carbon boat containing small volumes of supersaturated solutions, e.g. of GaP in Ga, as shown in Fig. 1.3. The solvent element (Ga or In) suppresses vacancies on sites of that element in the deposit. Lower growth temperatures can be obtained than for simple melts and growth rates can be high, but rough surfaces and interfaces can result and contamination by carry over of material from one melt to the next is possible. This technique worked surprisingly well in some cases but has largely fallen out of use now.

Molecular beam epitaxy (MBE) is a sophisticated form of evaporation in ultra high vacuum (see Fig. 1.43). Its relatively low growth temperatures make abrupt interfaces between different materials possible as little or no interdiffusion occurs during growth. It also allows continuous monitoring by methods taken from surface physics, such as reflection high-energy electron diffraction (RHEED), and good process control (for further details see Parker 1985, Herman and Sitter 1989 and Cho 1995).

Growth techniques, such as MBE and MOCVD, can produce structures in which layers of different materials and/or thicknesses (as small as a few monolayers) alternate. Such structures can have the characteristics of two-dimensional (2D) or one-dimensional (1D) quantum confined systems with novel properties, to be discussed below. The equipment used for MBE growth of multiquantum well (MQW) structures (for which purpose MBE was developed) is described in Section 1.7.3.

1.1.4 Crystal perfection

To minimize grown-in defects, crystals must be produced under controlled conditions to give, e.g. flat melt-crystal interfaces. Dash (1958) developed a Czochralski method of 'necking down' the seed crystal (Fig. 1.1), i.e. reducing the

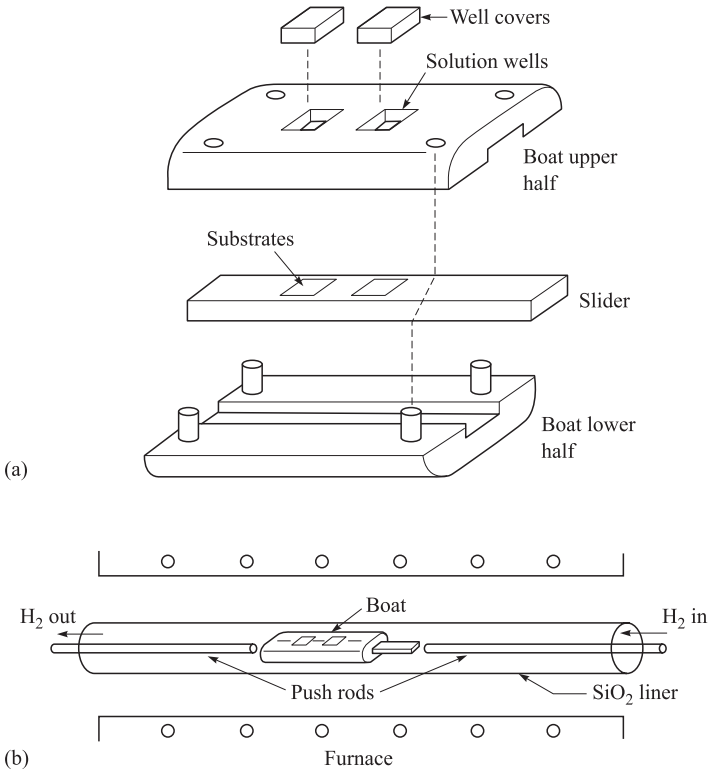

Figure 1.3 Liquid phase epitaxy equipment: (a) Construction of the boat and slider which are machined from reactor-grade graphite blocks. (b) The arrangement of the boat in the furnace. The substrates, held in the slider, are pushed under the melts, one after the other, to grow successive epitaxial layers. (After Sze 1985; *Semiconductor Devices: Physics and Technology*; Copyright 1985. Reprinted with permission of John Wiley & Sons, Inc.)

diameter by fast pulling. During necking down of the initial seed crystal the dislocations grew out the sides. Large, entirely dislocation-free crystals of Si, Ge and GaAs can be grown from such seeds. Structural defects reappear with each new material, and generally each new material at first exhibits some new type of defect in profusion. This requires research to identify the defects characteristic of the new material, their mechanism of generation and means of passivating (rendering electrically harmless) or eliminating them. At the time of writing this type of development is in progress in the case of GaN. New processing-induced defects, introduced into initially good material during device fabrication, including epitaxial growth, also keep appearing with each new device structure and production process.

To grow high perfection material by epitaxy the film and substrate materials must closely match in symmetry and lattice parameter at the interface. This ensures that the unit meshes in the two materials at the original growth surface match in shape

and size, respectively. This, in turn, allows low-energy bonding to occur across the interface. Symmetry mismatch opens the way for the formation of domains like the antiphase domains that can occur in a sphalerite-structure material such as GaAs grown on an (001)-oriented diamond-structure substrate such as Si. Lattice parameter matching minimizes the interface elastic strain, which favours misfit dislocation formation. However, for relatively small misfits, high-quality heterojunctions can be produced in pseudomorphic or strained-layer structures provided the epitaxially deposited layers are sufficiently thin. Then no misfit dislocations are generated at the interface and the lattice mismatch is accommodated by long-range elastic strain. Fig. 1.4(a) illustrates lattice-mismatched sphalerite-structure materials

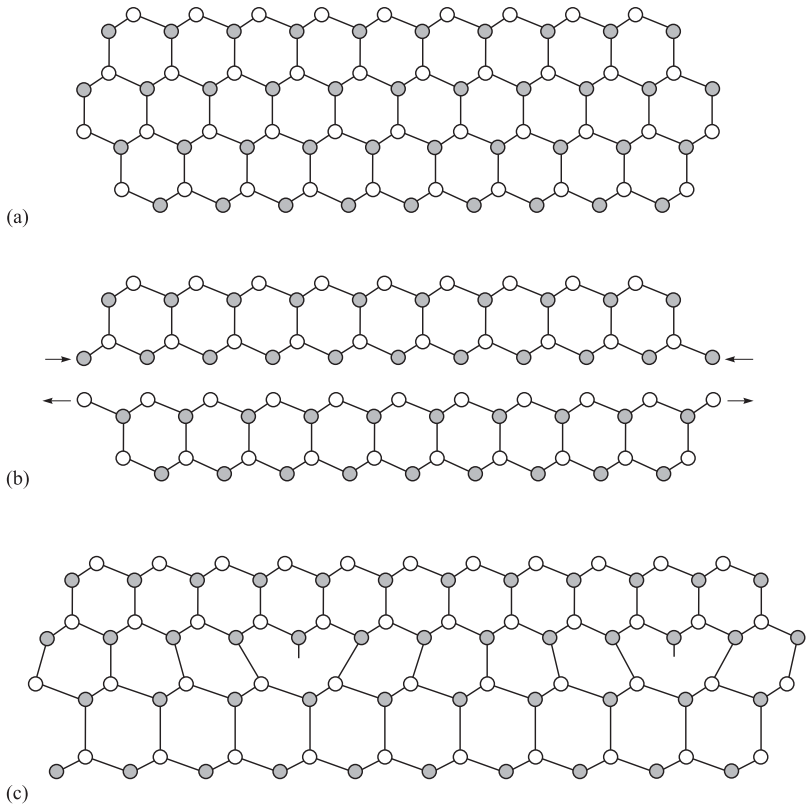

Figure 1.4 Misfit dislocations in a (111) heterojunction seen in projection on the $(01\bar{1})$ plane for the case in which the repeat distance $p = 5b = (5 + 1)a$. Here a and b are the lattice constants of the film (top) and substrate (bottom) respectively. (a) Perfect crystal of intermediate lattice parameter $\lambda = \lambda_1/2 + \lambda_2/2$. This is the reference structure. (b) The structure is cut along the (111) plane and expanded to λ_2 on one side and contracted to λ_1 on the other. (c) When the two crystals are bonded together there is a Vernier of period p. A dangling bond occurring at a spacing p marks the positions of successive misfit dislocations. (After Holt 1966.)

(envisaged as derived from an intermediate material by increasing the lattice constant of the substrate and decreasing that of the material of the film). The epitaxial heterostructures are shown with (Fig. 1.4b) the mismatch accommodated by long-range strain, and with (Fig. 1.4c) the mismatch accommodated by the localized strain at misfit dislocations. This will be discussed more fully in Section 4.6.

The historical advances in understanding the major mechanisms of formation of defects in semiconductor crystals were outlined by Hurle and Rudolph (2004) and Mahajan (2004). The former point out that dislocations can be eliminated in Si, but not in III-V and II-VI semiconductor compounds, in which the lower thermal conductivity and yield stresses prohibit sufficient reduction of the thermal stresses to prevent multiplication of dislocations (Hurle and Rudolph 2004).

1.1.5 Process-induced defects in devices

Differential contraction in the crystal due to thermal gradients during cooling after growth can lead to plastic deformation and introduce local dislocation densities greater than $10^6\,\mathrm{cm}^{-2}$. This is at least two orders of magnitude above the threshold for serious device effects in most semiconductors including silicon. Diffusion of dopant atoms of size different from the host Si atoms, notably B and P, produces strains. The resultant stresses can also cause slip and introduce 'diffusion-induced dislocations'. Heating during oxidation can produce stacking faults in silicon. Heating or diffusion in Si can produce impurity precipitates.

Dislocations can have large effects on semiconductor properties, so workers in industrial electronics laboratories played a major part in early, basic dislocation, research. W. Shockley and W. T. Read, then of the Bell Laboratories, for example, gave their names to Shockley partial dislocations and the Frank-Read dislocation source. As one result of this early work, material became available economically, with dislocation densities below the threshold level at which they ceased to be troublesome in discrete devices of Ge or Si and in the relatively large-sized constituent devices in early generations of Si integrated circuits (generally about $10^4\,\mathrm{cm}^{-2}$). Now industrial interest in process-induced defects in Si is limited because many problems can be solved with existing knowledge, trial and error and greater care in processing ('good housekeeping'). New materials, new methods of processing, smaller devices affected by fewer defects, and devices using more defect-sensitive properties, however, constantly raise new defect problems and re-arouse interest among industrial workers.

1.2 Electron energy levels and energy bands

The properties of semiconductors and defects depend on the way the wave functions and energies of electrons are influenced by the periodic potential in the perfect crystal