Testing of Digital Systems

Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over $40 billion a year. The most comprehensive and wide ranging book of its kind, *Testing of Digital Systems* covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through automatic test pattern generation, design for testability and built-in self-test of digital circuits before moving on to more advanced topics such as I_{DDQ} testing, functional testing, delay fault testing, CMOS testing, memory testing, and fault diagnosis. The book includes detailed treatment of the latest techniques including test generation for various fault models, discussion of testing techniques at different levels of the integrated circuit hierarchy and a chapter on system-on-a-chip test synthesis. Written for students and engineers, it is both an excellent senior/graduate level textbook and a valuable reference.

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To family and friends for their encouragement and understanding, to teachers and colleagues for sharing their wisdom, to students for sharing their curiosity.

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Preface

The fraction of the industrial semiconductor budget that manufacturing-time testing consumes continues to rise steadily. It has been known for quite some time that tackling the problems associated with testing semiconductor circuits at earlier design levels significantly reduces testing costs. Thus, it is important for hardware designers to be exposed to the concepts in testing which can help them design a better product. In this era of system-on-a-chip, it is not only important to address the testing issues at the gate level, as was traditionally done, but also at all other levels of the integrated circuit design hierarchy.

This textbook is intended for senior undergraduate or beginning graduate levels. Because of its comprehensive treatment of digital circuit testing techniques, it can also be gainfully used by practicing engineers in the semiconductor industry. Its comprehensive nature stems from its coverage of the transistor, gate, register-transfer, behavior and system levels of the design hierarchy. In addition to test generation techniques, it also covers design for testability, synthesis for testability and built-in self-test techniques in detail. The emphasis of the text is on providing a thorough understanding of the basic concepts; access to more advanced concepts is provided through a list of additional reading material at the end of the chapter.

The contents of the book are such that it contains all the material required for a first, one-semester, course in Testing (approximately 40 hours of teaching). The chapters are organized such that seven of the chapters contain mandatory material, while a selection from the remaining chapters may optionally be included.

Each chapter contains a set of exercises with different difficulty levels which can be used for in-class, as well as take-home exercises or tests.

In addition, the chapters contain many examples and a summary.

Chapter 1 introduces the readers to basic concepts in testing, such as faults, errors, tests, failure rate, fault coverage, and test economics.

Chapter 2 deals with fault models at various levels of the integrated circuit design hierarchy, e.g., behavioral, functional, structural, switch-level and geometric fault models. It also discusses different types of delay models, and inductive fault analysis.

Chapter 3 describes how fault-free and faulty circuit elements can be represented. It discusses a logic simulation algorithm and ways to accelerate logic simulation. It then proceeds to fault simulation, starting with well-known fault collapsing and

fault dropping concepts. It discusses the following fault simulation paradigms in detail: parallel fault simulation, parallel-pattern single-fault propagation simulation, deductive fault simulation, concurrent fault simulation, and critical path tracing. It also provides a brief background into approximate, low-complexity fault simulation approaches.

Chapter 4 covers test generation for combinational circuits. It starts with a discussion of composite circuit representation and value systems. Then it proceeds to basic concepts in test generation and implication procedures. Structural test generation algorithms and testability analysis techniques are targeted next. These include the *D*-algorithm, PODEM and their enhancements. Next, non-structural algorithms such as those based on satisfiability and binary decision diagrams are covered. Static and dynamic test compaction techniques and test generation algorithms for reduced heat and noise complete the chapter.

Chapter 5 deals with test generation for sequential circuits. It first classifies sequential test generation methods and faults. This is followed by discussion of fault collapsing and fault simulation. Test generation methods covered are those that start from a state table or gate-level implementation. Testing of asynchronous sequential circuits is also included. The chapter ends with a discussion of sequential test compaction methods.

Chapter 6 discusses I_{DDQ} testing. For combinational circuits, it targets testing of leakage faults and unrestricted bridging faults as well as test compaction. For sequential circuits, it targets test generation, fault simulation and test compaction. Under fault diagnosis, it covers analysis, diagnostic fault simulation and diagnostic test generation. It then introduces built-in current sensors. Under advanced I_{DDQ} testing concepts, it discusses i_{DD} pulse response testing, dynamic current testing, depowering, current signatures, and applicability of I_{DDQ} testing to deep submicron designs. It ends with a discussion on economics of I_{DDQ} testing.

Chapter 7 covers universal test sets, various types of pseudoexhaustive testing, and iterative logic array testing under the umbrella of functional testing.

Chapter 8 describes delay fault testing methods in detail. It first gives a classification of various types of delay faults. Then it provides test generation and fault simulation methods for combinational and sequential circuits containing the different types of delay faults. It also discusses some pitfalls of delay fault testing and how to overcome them. It closes with some advanced delay fault testing techniques.

Chapter 9 deals with test generation methods for static and dynamic CMOS circuits for stuck-open and stuck-on faults. It discusses the test invalidation problem for static CMOS circuits and design for testability methods to avoid them.

Chapter 10 covers fault diagnosis techniques. It includes both cause–effect and effect–cause diagnosis methods. It also discusses diagnostic test generation.

Chapter 11 describes design for testability methods. It discusses scan design, both full and partial, in considerable detail. It goes on to describe organization and use of

scan chains. It then discusses boundary scan. It finally describes design for testability techniques for delay faults and low heat dissipation.

Chapter 12 discusses built-in self-test (BIST) techniques. It starts with the basic concepts such as pattern generation, computation of test length, response compression, and aliasing analysis. It then proceeds to BIST methodologies, both in-situ and scan-based.

Chapter 13 concentrates on synthesis for testability techniques at the gate level. It covers many techniques under stuck-at and delay fault testability of combinational and sequential circuits.

Chapter 14 deals with memory testing. The topics covered are: reduced functional faults, traditional memory tests, March tests, pseudorandom memory tests, and BIST for embedded memories.

Chapter 15 discusses high-level test synthesis. It deals with the register-transfer and behavior levels of the design hierarchy. It describes hierarchical and high-level test generation techniques first. Then it discusses design for testability, synthesis for testability, and BIST techniques at the register-transfer and behavior levels.

Chapter 16 covers the modern topic of system-on-a-chip test synthesis. It discusses core-level test, core test access and core test wrappers.

The core chapters are Chapters 1, 2, 3, 4, 5, 11 and 12. These describe fault models, fault simulation and test generation for combinational and sequential circuits, design for testability and BIST. In a one semester course, if test generation needs to be emphasized, then this material can be augmented with a subset of Chapters 6, 7, 8, 9, 10 and 14. These chapters deal with I_{DDQ} testing, functional testing, delay fault testing, CMOS testing, fault diagnosis and memory testing, respectively. Alternatively, if synthesis for testability and testing at register-transfer, behavior and system levels need to be emphasized, the instructor can choose from Chapters 13, 15 and 16.

This book would not have been possible without help from many people. We first want to acknowledge Prof. Ad van de Goor who wrote the Introduction and Memory Testing chapters. We would like to thank our colleagues throughout the world who have used preprints of this book and given valuable feedback. These include Profs. S. Blanton, K.-T. Cheng, S. Dey, D. Ha, J. P. Hayes, J. Jacob, P. Mazumder, I. Pomeranz, D. Pradhan, S. M. Reddy, and S. Seth. We are indebted to our copy editor, F. Nex, who discovered some latent bugs. Finally, our thanks go to the students at Princeton University and University of Southern California who helped make the book better through their helpful suggestions.

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Gate symbols