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THREE-DIMENSIONAL INTEGRATED CIRCUIT LAYOUT

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To my parents
Abstract

Some recent developments in semiconductor process technology have made possible the construction of three-dimensional integrated circuits. Unlike other technological developments in two-dimensional integration, these circuits present a new and inherently richer connection topology. This offers the potential for improved layout in terms of increased density and reduced interconnect length. These circuits will be difficult and expensive to manufacture, at least in the short term, and the scale of the improvement in layout is not apparent. This dissertation presents a discussion of layout and design for three-dimensional integrated circuits.

A number of materials and techniques can be used in the manufacture of such circuits. This choice has a profound bearing on the topology of circuit layout. A classification relating process technology to layout topology is developed and illustrated with the design of a number of circuits. A layout system is presented as the vehicle for a series of experiments in three-dimensional layout. It is shown that the system can be constrained to perform circuit layout in a number of topologies in the classification.

Finally, some attempt to quantify the benefits of three-dimensional layout is made. The layout model is calibrated by designing examples of basic circuit elements. This is done using a set of design rules corresponding to a proposed three-dimensional process technology. Circuit layouts produced by the system are compared with conventional two-dimensional layouts, and the variation in layout quality as a function of the three-dimensionality of a layout is explored.
Preface

I am indebted to my supervisor, Andy Hopper, for his encouragement and support. He first introduced me to the topic of computer aided design of integrated circuits when I was an undergraduate, and has been a source of guidance ever since. I am also indebted to Roger Needham for extending the facilities of the Computer Laboratory. I am grateful that both Andy and Roger have demonstrated quite remarkable patience. The Science and Engineering Research Council provided funding for three years for which I am thankful.

Of the many people who have been a source of help, I would particularly like to thank David Wheeler for a number of stimulating discussions, and Haroon Ahmed of the Microcircuit Engineering Laboratory for introducing me to the technology of three-dimensional circuits. Alan Mathewson and Ciaran Cahill, of the National Microelectronics Research Centre, University College, Cork, have contributed to my further understanding of the technological possibilities. Elements of the systems used in the case study described in chapter two were developed by myself, Jeremy Dion, Alan Jones, Tony Mann, Trevor Morris, John Porter, Peter Robinson and Chris Stenton. I would like to thank Tony Mann and John Porter for reminding me about the details of the placement and routing schemes.

Chris Stenton and Steve Temple have contributed many helpful suggestions particularly in the experimental stages and were diligent proof readers, as were Tim Cole and David Greaves. I am grateful for their suggestions for improvements.

This dissertation is the result of my own work and is not the outcome of any work done in collaboration. I declare that this dissertation is not the same as any other dissertation I have submitted for a degree, diploma or other qualification at any university. Furthermore, no part of this dissertation has been or is currently being submitted for any such qualification.
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Glossary of Terms

The number of the page on which the term is introduced appears in parentheses after each term.

FET        Field-effect transistor (4).
MOS        Metal-oxide-semiconductor (4).
NMOS       n-type metal-oxide-semiconductor (4).
PMOS       p-type metal-oxide-semiconductor (4).
CMOS       Complementary-metal-oxide-semiconductor (5).
CAD        Computer-aided design (5).
SRAM       Static random-access memory (5).
DRAM       Dynamic random-access memory (11).
SSI        Small-scale integration (11).
MSI        Medium-scale integration (11).
LSI        Large-scale integration (11).
VLSI       Very-large-scale integration (11).
WSI        Wafer-scale integration (11).
FIFO       First-in first-out (20).
HDL        Hardware Description Language (24).
GLOSSARY OF TERMS

CFR  Cambridge Fast Ring (28).

ASIC  Application Specific Integrated Circuit (29).

SOI  Silicon on insulator (35).

CVD  Chemical Vapour Deposition (38).